PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2003-046061
(43)Date of publication of application : 14.02.2003

(51)Int.Cl. H01L 25/16

(21)Application number : 2001-284049
(22)Date of filing : 18.09.2001

(71)Applicant : IBIDEN CO LTD
(72)Inventor : TANAKA HIRONORI
ASAI MOTOO

(30)Priority
Priority number : 2001157858 Priority date : 25.05.2001 Priority country : JP

(54) SUBSTRATE FOR MOUNTING IC CHIP

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a substrate for mounting an IC chip which is a component for optical communication, in which an IC chip and an optical component are formed integratedly, the distance between the IC chip and the optical component is short, and reliability regarding electrical signal transmission is superior.
SOLUTION: In this substrate for mounting IC chip, an optical wiring layer, having a region for mounting an optical element, is laminated on a package substrate where conductor circuits and interlayer resin insulating layers are laminated and formed on both surfaces of a substrate. On the region for mounting an optical element, an optical element is arranged, and a resin-filled layer is formed. The optical element is electrically connected with the package substrate. The resin-filled layer is constituted of at least two layers which are a lower resin-filled layer, whose thickness is the same as that of the optical element or smaller than that of the optical element, and an upper resin-filled layer which is laminated and formed on the lower resin-filled layer.

LEGAL STATUS
[Date of request for examination]
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The laminating of the optical wiring layer which has a field for optical element mounting on the package substrate with which it comes to carry out laminating formation of a circuit and the resin insulating layer between layers is carried out. both sides of a substrate — a conductor — in said field for optical element mounting It is the substrate for IC chip mounting to which a resin packed bed is formed in while an optical element is arranged, and said optical element and said package substrate are connected electrically. Said resin packed bed The substrate for IC chip mounting with which the thickness is characterized by the thing with the upper resin packed bed by which is the same as the thickness of said optical element, or laminating formation was carried out on the lower layer resin packed bed thinner than the thickness of said optical element, and said lower layer resin packed bed consisted of two-layer at least.
[Claim 2] Said upper resin packed bed is a substrate for IC chip mounting according to claim 1 whose transmission of the communication link wavelength light of the perpendicular direction between the top face and inferior surface of tongue is 90% or more.
[Claim 3] Said upper resin packed bed is a substrate for IC chip mounting according to claim 1 whose transmission of the communication link wavelength light per die length of 1mm is 90% or more.
[Claim 4] Said optical element and said package substrate are a substrate for IC chip mounting according to claim 1, 2, or 3 electrically connected by wirebonding.
[Claim 5] Said optical element is a substrate for IC chip mounting according to claim 4 with which the pad for electrical connection is formed in the location lower than a light sensing portion or a light-emitting part.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the substrate for IC chip mounting.
[0002]
[Description of the Prior Art] In recent years, attentions have gathered for the optical fiber focusing on the communication link field. In especially IT (information technology) field, the communication technology which used the optical fiber for maintenance of the high-speed Internet network is needed. In the communication system using the optical fiber which has the descriptions, such as ** low loss, ** high bandwidth, ** narrow diameter and a light weight, no ** guiding, and ** saving resources, and has this description, compared with the communication system using the conventional metallic cable, the number of repeaters can be reduced sharply, construction and maintenance become easy, and an optical fiber can attain economization of communication system, and high-reliability-ization.
[0003] Moreover, since an optical fiber can multiplex the light of the wavelength from which not only the light of one wavelength but many differ to coincidence with one optical fiber, it can realize the transmission line of the large capacity which can respond to a busy application, and can respond to image service etc.
[0004] Then, in network communication, such as such the Internet, using not only for the communication link of a backbone but for the communication link with a backbone and terminal equipments (a personal computer, mobile one, game, etc.) and the communication link of terminal equipments the optical communication used with the optical fiber is proposed.
[0005] Thus, when using optical communication for the communication link with a backbone and a terminal equipment etc., in order for IC which performs information (signal) processing in a terminal equipment to operate with an electrical signal, it is necessary to attach the equipment (henceforth light/electric transducer) which changes the lightwave signal and electrical signal of optical -> electric transducer, electric -> phototransducer, etc. into a terminal equipment. So, in the conventional terminal equipment, for example, optics, such as a substrate which mounted IC chip, a photo detector which processes a lightwave signal, and a light emitting device, etc. were mounted separately, electric wiring and optical waveguide were connected to these, and a signal transmission and signal processing were performed.
[0006]
[Problem(s) to be Solved by the Invention] In such a conventional terminal equipment, since IC mounting package substrate and the optic were mounted separately, the whole equipment became large and had become the factor which bars the miniaturization of a terminal equipment. Moreover, in the conventional terminal equipment, since the distance of IC mounting package substrate and an optic was separated, electric wiring distance is long and it was easy to generate the signal error by a cross talk noise etc. at the time of a signal transmission.
[0007]
[Means for Solving the Problem] Then, while attaining the optical communication which is excellent in connection dependability, as a result of examining wholeheartedly the substrate for IC chip mounting which can be contributed to the miniaturization of a terminal equipment, by mounting various optics in the substrate for IC chip mounting, this invention person etc. hit on an idea for the technical problem mentioned above to be solvable, and completed the substrate for IC chip mounting of this invention which consists of the following configuration.
[0008] namely, the substrate for IC chip mounting of this invention — both sides of a substrate — a conductor — a circuit and the resin insulating layer between layers on the package substrate which comes to carry out laminating formation The laminating of the optical wiring layer which has a field for optical element mounting is carried out. In the above-mentioned field for optical element mounting It is the substrate for IC chip mounting to

which a resin packed bed is formed in while an optical element is arranged, and the above-mentioned optical element and the above-mentioned package substrate are connected electrically. The above-mentioned resin packed bed The thickness is the same as the thickness of the above-mentioned optical element, or is characterized by the thing of a lower layer resin packed bed thinner than the thickness of the above-mentioned optical element, and the upper resin packed bed by which laminating formation was carried out on the above-mentioned lower layer resin packed bed consisted of two-layer at least.

[0009] Moreover, in the substrate for IC chip mounting of this invention, as for the above-mentioned upper resin packed bed, it is desirable for the permeability of the communication link wavelength light of the perpendicular direction between the top face and inferior surface of tongue to be 90% or more, and it is desirable for the permeability of the communication link wavelength light per die length of 1mm to be also 90% or more.

[0010] Moreover, in the above-mentioned substrate for IC chip mounting, as for the above-mentioned optical element and the above-mentioned package substrate, it is desirable for wirebonding to connect electrically, and, as for the above-mentioned optical element, it is more desirable to be formed in the location where the pad for electrical connection is lower than a light sensing portion or a light-emitting part in this case.

[0011]

[Embodiment of the Invention] the substrate for IC chip mounting of this invention — both sides of a substrate -- a conductor — a circuit and the resin insulating layer between layers on the package substrate which comes to carry out laminating formation The laminating of the optical wiring layer which has a field for optical element mounting is carried out. In the above-mentioned field for optical element mounting It is the substrate for IC chip mounting to which a resin packed bed is formed in while an optical element is arranged, and the above-mentioned optical element and the above-mentioned package substrate are connected electrically. The above-mentioned resin packed bed The thickness is the same as the thickness of the above-mentioned optical element, or is characterized by the thing of a lower layer resin packed bed thinner than the thickness of the above-mentioned optical element, and the upper resin packed bed by which laminating formation was carried out on the above-mentioned lower layer resin packed bed consisted of two-layer at least.

[0012] With the substrate for IC chip mounting of this invention, since the optical element is mounted in that interior, when IC chip is mounted in this substrate for IC chip mounting, the distance of IC chip and an optic is short and it excels in the dependability of electrical signal transmission. Moreover, in the above-mentioned substrate for IC chip mounting, since electronic parts and an optic required for optical communication can be unified, it can contribute to the miniaturization of the terminal equipment for optical communication.

[0013] Hereafter, it explains, referring to a drawing about the substrate for IC chip mounting of this invention. Drawing 1 is the sectional view showing typically 1 operation gestalt of the substrate for IC chip mounting of this invention. In addition, drawing 1 shows the substrate for IC chip mounting in the condition that IC chip was mounted.

[0014] it is shown in drawing 1 — as — the substrate 100 for IC chip mounting — both sides of a substrate 121 — a conductor — the conductor with which laminating formation was carried out and the substrate 121 of the resin insulating layer [a circuit 124 and] 122 between layers was pinched — the laminating of the optical wiring layer 120 which has an optical element mounting field on the package substrate 160 to which the circuit is connected by the through hole 129 is carried out. the optical wiring layer 120 — both sides of a substrate 101 -- a conductor — a circuit forms — having — this — a conductor — the through hole 106 which connects between circuits is formed, and, as for this through hole 106, the resin filler layer 110 is formed in that interior, and the wrap lid plating layer 116 is formed in that upper part in the resin filler layer 110.

[0015] Moreover, the optical wiring layer 120 has the field for optical element mounting in the center of abbreviation. While the optical element of a photo detector 138 and a light emitting device 139 is arranged in this field for optical element mounting, a resin packed bed (lower layer resin packed bed 141a, upper resin packed bed 141b) is formed in it, and the above-mentioned optical element is electrically connected with the metal layers 136a and 136b of the package substrate 160 by wirebonding through a wire 140. Moreover, a resin packed bed consists of two-layer [of lower layer resin packed bed 141a with the thickness thinner than the thickness of an optical element (a photo detector 138 and light emitting device 139), and upper resin packed bed 141b by which laminating formation was carried out on lower layer resin packed bed 141a].

[0016] In addition, in the substrate 100 for IC chip mounting shown in drawing 1, although the thickness of lower layer resin packed bed 141a is thinner than the thickness of an optical element, the thickness of a lower layer resin packed bed may be the same as the thickness of an optical element. Moreover, in the substrate 100 for IC chip mounting, the resin packed beds 141a and 141b, optical elements 138 and 139, and the field that a wire 140 occupies are equivalent to the field for optical element mounting. Moreover, although the resin packed bed consists of two-layer [of lower layer resin packed bed 141a and upper resin packed bed 141b] in the substrate 100 for IC chip mounting, the number of layers of a resin packed bed is not limited to two-layer, and the lower

layer resin packed bed and the upper resin packed bed may consist of more than two-layer, respectively.
[0017] Moreover, the solder resist layers 134 and 154 to which the substrate 100 for IC chip mounting has opening in the outermost layer are formed, and the solder bump 157 for flip chips and the solder bump 158 for BGA are formed in opening of the solder resist layers 134 and 154 through the solder pads (metal layer) 136 and 156.
[0018] As an optical element arranged in the above-mentioned field for optical element mounting, light emitting devices, such as photo detectors, such as PD (photodiode) and APD (avalanche photodiode), LD (semiconductor laser), DFB-LD (distribution feedback mold-semiconductor laser), and LED (light emitting diode), etc. are mentioned, for example.
[0019] As an ingredient of the above-mentioned photo detector, Si, germanium, InGaAs, etc. are mentioned, for example. In these, a point to InGaAs which is excellent in light-receiving sensibility is desirable. Moreover, as an ingredient of the above-mentioned light emitting device, a gallium, arsenic and the compound (GaAsP) of Lynn, a gallium, aluminum and the compound (GaAlAs) of arsenic, a gallium and the compound (GaAs) of arsenic, an indium, a gallium and the compound (InGaAs) of arsenic, an indium, a gallium, arsenic, the compound (InGaAsP) of Lynn, etc. are mentioned, for example. That what is necessary is just to use these properly in consideration of communication link wavelength, when communication link wavelength is 0.85-micrometer band, GaAlAs can be used, and in the case of 1.3-micrometer band or 1.55-micrometer band, communication link wavelength can use InGaAs and InGaAsP.
[0020] In the substrate 100 for IC chip mounting which consists of such a configuration The lightwave signal sent from the outside through an optical fiber, optical waveguide (not shown), etc. After receiving by the photo detector 138 (light sensing portion 138a), it is changed into an electrical signal by the photo detector 138. furthermore, metal layer 136a-Bahia hall 127a-through hole 129a — it will be sent to the IC chip 180 through solder bump 157a for - Bahia hall 127b-flip chips, and will be processed with the IC chip 180.
[0021] moreover, the electrical signal sent out from the IC chip 180 — the object for flip chips — after being sent to a light emitting device 139 through solder bump 157b-Bahia hall 127c-through hole 129b-Bahia hall 127d-metal layer 136b, it will be changed into a lightwave signal by the light emitting device 139, and this lightwave signal will be sent to optical waveguide or an optical fiber from a light emitting device 139 (light-emitting part 139a).
[0022] In such a substrate for IC chip mounting of a configuration, in the photo detector and light emitting device which were mounted in the location near IC chip, since light / electrical signal conversion is performed, the transmission distance of an electrical signal is short, is excellent in the dependability of a signal transmission, and can respond to a high-speed communication link more.
[0023] Moreover, in the above-mentioned substrate for IC chip mounting, the thickness of a lower layer resin packed bed is the same as the thickness of an optical element, or thinner than it. Therefore, as for a lower layer resin packed bed, it is desirable to be formed using the resin (hard resin and resin which is excellent in thermal resistance) which is excellent in the property of protecting the connection part of wirebonding and a package substrate.
[0024] Therefore, as an ingredient of the above-mentioned lower layer resin packed bed, the same thing as the ingredient of the well-known resin for IC chip closures etc. is mentioned for example, conventionally. The resin constituent which specifically contains the resin complex of thermosetting resin, thermoplastics, a photopolymer, the resin with which some thermosetting resin was photosensitivity-ized, thermosetting resin, and thermoplastics, the complex of a photopolymer and thermoplastics, etc. is mentioned. As an example, as a filler, a silica etc. is blended with phenol novolak system resin as a curing agent, it is blended with the epoxy resin of a clay ZORU novolak system, and the resin constituent with which the additive of others, such as a reaction accelerator, a coupling agent, a flame retarder (fire-resistant assistant), and a coloring agent, was blended is mentioned further if needed, for example.
[0025] On the other hand, since this upper resin packed bed serves as a transmission route of a lightwave signal, as for the upper resin packed bed, it is desirable to be formed using the resin which is excellent in the permeability of communication link wavelength light. Therefore, the resin constituent which uses as a resinous principle thermosetting resin, thermoplastics, a photopolymer, the resin with which some thermosetting resin was photosensitivity-ized, these complex, etc. as the ingredient, for example is mentioned. As an example of the above-mentioned resinous principle, an epoxy resin, phenol resin, polyimide resin, olefine resin, BT resin, etc. are mentioned, for example. Moreover, particles, such as for example, a resin particle, an inorganic particle, and metal particles, may be contained in the above-mentioned resin constituent in addition to the above-mentioned resinous principle. By including these particles, adjustment of a coefficient of thermal expansion can be aimed at between a resin packed bed, a substrate and a solder resist layer, the resin insulating layer between layers, etc., and fire retardancy can also be given depending on the class of particle.

[0026] What consists of resin complex of thermosetting resin, thermoplastics, a photopolymer, the resin with which some thermosetting resin was photosensitivity-ized, thermosetting resin, and thermoplastics, complex of a photopolymer and thermoplastics, etc. as the above-mentioned resin particle, for example is mentioned.
[0027] Specifically For example, an epoxy resin, phenol resin, polyimide resin, Thermosetting resin, such as a bismaleimide resin, polyphenylene resin, polyolefin resin, and a fluororesin; The heat-curing radical of these thermosetting resin A methacrylic acid, an acrylic acid, etc. are made to react to (for example, the epoxy group in an epoxy resin). Resin which gave the acrylic radical; Phenoxy resin, polyether sulfone (PES), Thermoplastics, such as polysulfone (PSF), a polyphenylene sulfone (PPS), polyphenylene sulfide (PPES), a polyphenyl ether (PPE), and polyether imide (PI); what consists of photopolymers, such as acrylic resin, etc. is mentioned. Moreover, what consists of resin complex of the resin complex of the above-mentioned thermosetting resin and the above-mentioned thermoplastics, the resin which gave the above-mentioned acrylic radical, the above-mentioned photopolymer, and the above-mentioned thermoplastics can also be used. Moreover, the resin particle which consists of rubber can also be used as the above-mentioned resin particle.
[0028] Moreover, as the above-mentioned inorganic particle, what consists of titanium compounds, such as silicon compounds, such as magnesium compounds, such as potassium compounds, such as lime compounds, such as aluminium compounds, such as an alumina and an aluminum hydroxide, a calcium carbonate, and a calcium hydroxide, and potassium carbonate, a magnesia, a dolomite, and basic magnesium carbonate, a silica, and a zeolite, and a titania, etc. is mentioned, for example. Moreover, what consists of Lynn or phosphorus compounds can also be used as the above-mentioned inorganic particle.
[0029] As the above-mentioned metal particles, what consists of Au, Ag, Cu, Pd, nickel, Pt, Fe, Zn, Pb, aluminum, Mg, calcium, etc. is mentioned, for example. These resin particles, an inorganic particle, and metal particles may be used independently, respectively, and may be used together two or more sorts.
[0030] Moreover, especially the configuration of the above-mentioned particle is not limited, for example, the shape of a globular shape, an ellipse globular shape, the letter of crushing, and a polyhedron etc. is mentioned. Moreover, as for the particle size (the die length of the longest part of a particle) of the above-mentioned particle, it is desirable that it is shorter than the wavelength of communication link light. It is because transmission of a lightwave signal may be checked when particle size is longer than the wavelength of communication link light.
[0031] Moreover, as for the upper resin packed bed formed using the above-mentioned resin constituent, it is desirable for the permeability of the communication link wavelength light of the perpendicular direction between the top face and inferior surface of tongue to be 90% or more. In addition, in this specification, the permeability (%) of the communication link wavelength light between the top face of a resin packed bed and an inferior surface of tongue is a value computed from the following formula (1), when the intensity of light which passed I1 and the above-mentioned upper resin packed bed, and came out of the strength of the incident light of the perpendicular direction to the above-mentioned upper resin packed bed is set to I2.
[0032]
Permeability (%) =(I2/I1) x100 ... (1)
[0033] Moreover, as for the upper resin packed bed, it is desirable for the permeability of the communication link wavelength light per die length of 1mm to be also 90% or more. When the thickness of the resin packed bed formed at this process is taken into consideration, the resin packed bed which has the permeability of the above-mentioned range is because it fully excels in the transmission nature of communication link light.
[0034] In addition, in this specification, the permeability (%) of the communication link wavelength light per die length of 1mm is a value computed by the following formula (2), when the light of I3 carried out incidence to the above-mentioned upper resin packed bed in strength, and passing this upper resin packed bed 1mm, having come out and the intensity of light which came out is I4.
[0035]
Permeability (%) =(I4/I3) x100 ... (2)
[0036] Moreover, as it is in the substrate 100 for IC chip mounting, in the substrate for IC chip mounting of this invention, it is desirable for connection between the above-mentioned optical element and the above-mentioned package substrate to be made by wirebonding. It is because it is economically advantageous while this has the large degree of freedom of the design at the time of attaching an optical element.
[0037] Moreover, when making connection between an optical element and a package substrate by wirebonding, as for the above-mentioned optical element, what is formed in the location where the pad for electrical connection is lower than a light sensing portion or a light-emitting part (the formation location of the pad for electrical connection means that it is a package substrate side from the formation location of a light sensing portion or a light-emitting part) is desirable (refer to drawing 2).
[0038] Since the connection of the pad for electrical connection and a wire can also be protected by the lower

layer resin packed bed by using the optical element by which such a pad for electrical connection is formed in the location lower than a light sensing portion or a light-emitting part, it can consider as the multilayer printed wiring board which is more excellent in connection dependability. The substrate for IC chip mounting using the optical element by which such a pad for electrical connection is formed in the location lower than a light sensing portion or a light-emitting part is explained below, referring to a drawing.

[0039] Drawing 2 is the sectional view showing typically 1 another operation gestalt of the substrate for IC chip mounting of this invention. The optical element of the above-mentioned configuration is attached in drawing 2 , and the substrate for IC chip mounting of a gestalt with which the through hole which penetrates an optical wiring layer and a package substrate was formed is shown.

[0040] the substrate 200 for IC chip mounting — both sides of a substrate 221 — a conductor — the conductor with which laminating formation was carried out and the substrate 221 of the resin insulating layer [a circuit 224 and] 222 between layers was pinched — the laminating of the optical wiring layer 220 which has an optical element mounting field on the package substrate 260 to which the circuit is connected by the through hole 129 is carried out.

[0041] Moreover, the optical wiring layer 220 has the field for optical element mounting in the center of abbreviation. While the optical element of a photo detector 238 and a light emitting device 239 is arranged in this field for optical element mounting, a resin packed bed (lower layer resin packed bed 241a, upper resin packed bed 241b) is formed in it, and the above-mentioned optical element is electrically connected with the metal layer 236 (236a, 236b) of the package substrate 260 by wirebonding through a wire 240. Moreover, the pads 1238 and 1239 for electrical connection of a photo detector 238 and a light emitting device 239 are formed in the location respectively lower than light sensing portion 238a and light-emitting part 239a. Therefore, the connection of the pads 1238 and 1239 for electrical connection and a wire 240 will also be protected by lower layer resin packed bed 241a.

[0042] Moreover, a resin packed bed consists of two-layer [of lower layer resin packed bed 241a with the thickness thinner than the thickness of an optical element (a photo detector 238 and light emitting device 239), and upper resin packed bed 241b by which laminating formation was carried out on lower layer resin packed bed 241a] in the substrate 200 for IC chip mounting. In addition, in the substrate 200 for IC chip mounting, although the thickness of the lower layer resin packed bed 241 is thinner than the thickness of an optical element, the thickness of a lower layer resin packed bed may be the same as the thickness of an optical element. In addition, in the substrate 200 for IC chip mounting, the resin packed beds 241a and 241b, optical elements 238 and 239, and the field that a wire 240 occupies are equivalent to the field for optical element mounting.

[0043] Moreover, the through hole 249 which penetrates the optical wiring layer 220 and the package substrate 260 is formed, and the resin filler layer 250 is filled up with the substrate 200 for IC chip mounting into the interior. moreover, the solder resist layers 234 and 254 which have opening in the outermost layer form the substrate 200 for IC chip mounting — having — **** — opening of the solder resist layers 234 and 254 — metal layer 236a — it 236b minds and the solder bump 257 for flip chips and the solder bump 258 for BGA are formed.

[0044] Like the substrate 100 for IC chip mounting shown in drawing 1 , such a substrate 200 for IC chip mounting of a configuration is excellent in the dependability of a signal transmission, and since the connection of an optical element and a wire is also protected by the lower layer resin packed bed in addition to the ability to respond to a high-speed communication link more, it is more excellent in dependability.

[0045] Moreover, like the substrate for IC chip mounting shown in drawing 1 or drawing 2 , when the solder bump is formed in the solder resist layer by the side of the above-mentioned optical wiring layer, the above-mentioned substrate for IC chip mounting can be connected with an external substrate through a solder bump, and the above-mentioned substrate for IC chip mounting can be arranged to a position in this case according to the self-alignment operation which solder has.

[0046] In addition, in order that, as for a self-alignment operation, a solder resist layer may crawl solder, solder says the operation to which it is going to exist in a stable configuration by near the center of opening for solder bump formation with the fluidity which self has at the time of reflow processing. Though location gap has occurred to both in front of a reflow in case the above-mentioned substrate for IC chip mounting is connected to an external substrate through the above-mentioned solder bump when this self-alignment operation is used, the above-mentioned substrate for IC chip mounting can move at the time of a reflow, and this substrate for IC chip mounting can be attached in the exact location on an external substrate. Therefore, if the mounting position of the photo detector mounted in the above-mentioned substrate for IC chip mounting or an optical element is exact when transmitting a lightwave signal through the photo detector and light emitting device which were mounted in the above-mentioned substrate for IC chip mounting, and the optics (optical waveguide etc.) mounted in the above-mentioned external substrate, an exact lightwave signal can be transmitted between the

above-mentioned substrate for IC chip mounting, and the above-mentioned external substrate.
[0047] Next, how to manufacture the substrate for IC chip mounting of this invention is explained. Manufacture of the substrate for IC chip mounting of this invention performs both by passing through lamination and a further predetermined process, after producing separately for example, a package substrate and an optical wiring layer. Therefore, how to produce an optical wiring layer and the approach of producing a package substrate are first explained separately in order of a process, respectively, and the process which sticks both and is used as the substrate for IC chip mounting is explained after that here.
[0048] Production of a package substrate can be performed by passing through the process of for example, following (A) - (C).
(A) first — a substrate top — a conductor — form a circuit. performing etching processing, after forming a solid conductor layer by nonelectrolytic plating processing etc. on a substrate and specifically forming a resist on this conductor layer — a substrate top — a conductor — a circuit is formed. moreover, the thing for which plating resist is formed on a substrate and plating processing and exfoliation of plating resist are performed after that — a substrate top — a conductor — a circuit may be formed.
[0049] As the above-mentioned substrate, the substrate with which reinforcing materials, such as a glass fiber, consist of resin (for example, glass epoxy resin) with which it sank in, FR-4 substrate, FR-5 substrate, etc. are mentioned to an epoxy resin, polyester resin, polyimide resin, bismaleimide-triazine resin (BT resin), phenol resin, and these resin, for example. Moreover, a double-sided copper-clad laminated circuit board, an one side copper-clad laminated circuit board, a RCC substrate, etc. may be used as a substrate with which the solid conductor layer was formed. in addition, a conformal substrate and the substrate formed with the additive process — a conductor — you may use as a substrate with which the circuit was formed.
[0050] moreover, the conductor whose above-mentioned substrate was pinched if needed — the through hole which connects between circuits may be formed. the case where a through hole is formed — for example, the thing, for which a conductor layer is formed also in the wall surface of a through tube in case the through tube is formed in the substrate by drilling, the lasing, etc. and a solid conductor layer is formed beforehand, before forming a solid conductor layer, and etching processing is performed after that — a conductor — what is necessary is just to form a through hole, while forming a circuit moreover, the thing for which nonelectrolytic plating processing etc. is performed to the wall surface of this through tube, and etching processing is further performed to a conductor layer after forming a through tube in the substrate with which the solid conductor layer was formed beforehand — a conductor — a circuit and a through hole may be formed.
[0051] Moreover, when a through hole is formed, it is desirable to be filled up with a resin filler in this through hole. In addition, restoration of a resin filler can lay on a substrate the mask with which opening was formed in the part equivalent to a through hole, and can be performed using a squeegee.
[0052] moreover, a conductor — roughening formation processing may be performed to a circuit front face (the land front face of a through hole is included). a conductor — it is because adhesion with the resin insulating layer between layers which carries out laminating formation at a back process by making a circuit front face into a roughening side can be raised. as the above-mentioned roughening formation processing — melanism (oxidization) — the etching processing using the etching reagent containing - reduction processing, the second copper complex, and an organic-acid salt etc., processing by the Cu-nickel-P needlelike alloy plating, etc. are mentioned. In addition, before this roughening formation processing is filled up with a resin filler in a through hole, it may be performed, and it may form a roughening side also in the wall surface of a through hole. It is because the adhesion of a through hole and a resin filler improves.
[0053] As a resin filler with which it is filled up in the above-mentioned through hole, the resin constituent containing an epoxy resin, a curing agent, and an inorganic particle etc. is mentioned, for example. Although not limited especially as the above-mentioned epoxy resin, a kind is [choose / from the group which consists of a bisphenol mold epoxy resin and a novolak mold epoxy resin] desirable in it being few. It is because a novolak mold epoxy resin is excellent in thermal resistance or chemical resistance with high intensity, the viscosity can be prepared even if a diluent solvent is not used for a bisphenol mold epoxy resin by choosing the resin of A mold or a female mold, it is not disassembled even if it is among strong base nature solutions, such as nonelectrolytic plating liquid, and it is hard to carry out a pyrolysis.
[0054] As the above-mentioned bisphenol mold epoxy resin, the bisphenol A mold epoxy resin and a bisphenol female mold epoxy resin are desirable, and the point which is hypoviscosity and can be used with a non-solvent to a bisphenol female mold epoxy resin is more desirable. Moreover, as the above-mentioned novolak mold epoxy resin, a kind is [choose / from a phenol novolak mold epoxy resin and a cresol novolak mold epoxy resin] desirable in it being few.
[0055] Moreover, a bisphenol mold epoxy resin and a cresol novolak mold epoxy resin may be mixed and used. In this case, as for the mixed ratio of a bisphenol mold epoxy resin and a cresol novolak mold epoxy resin, it is

desirable that it is 1 / 1 - 1/100 in a weight ratio.

[0056] It is not limited especially as a curing agent contained in the above-mentioned resin filler, a well-known curing agent can be used conventionally, for example, an imidazole system curing agent, an acid-anhydride curing agent, an amine system curing agent, etc. are mentioned. In these, an imidazole system curing agent is desirable and liquefied 1-benzyl-2-methylimidazole, and 1-cyanoethyl-2-ethyl-4-methylimidazole and a 4-methyl-2-ethyl imidazole are desirable in 25 degrees C especially.

[0057] Moreover, as an inorganic particle contained in the above-mentioned resin filler, what consists of titanium compounds, such as silicon compounds, such as magnesium compounds, such as potassium compounds, such as lime compounds, such as aluminium compounds, such as an alumina and an aluminum hydroxide, a calcium carbonate, and a calcium hydroxide, and potassium carbonate, a magnesia, a dolomite, basic magnesium carbonate, and talc, a silica, and a zeolite, and a titania, etc. is mentioned, for example. These may be used independently and may be used together two or more sorts. Moreover, coating of the above-mentioned inorganic particle may be carried out by the silane coupling agent etc. It is because the adhesion of an inorganic particle and an epoxy resin improves.

[0058] Moreover, the content ratio in the resin constituent of the above-mentioned inorganic particle has 10 - 80 desirable % of the weight, and its 20 - 70 % of the weight is more desirable. It is because adjustment of a coefficient of thermal expansion can be aimed at between substrates etc. if it is this range.

[0059] Moreover, especially the configuration of the above-mentioned inorganic particle is not limited, but the shape of a globular shape, an ellipse globular shape, the letter of crushing, and a polyhedron etc. is mentioned. In these, the shape of the shape of a ball or an ellipse ball is desirable. It is because generating of the crack resulting from the configuration of a particle etc. can be controlled. The mean particle diameter of the above-mentioned inorganic particle has desirable 0.01-5.0 micrometers.

[0060] Moreover, in the above-mentioned resin constituent, other thermosetting resin, thermoplastics, etc. may be contained in addition to the above-mentioned epoxy resin etc. As the above-mentioned thermosetting resin, polyimide resin, phenol resin, etc. are mentioned, for example. As the above-mentioned thermoplastics For example, a polytetrafluoroethylene (PTFE) and ethylene tetrafluoride 6 fluoride propylene copolymer (FEP), Fluororesins, such as an ethylene tetrafluoride perphloro alkoxy copolymer (PFA), Polyethylene terephthalate (PET), polysulfone (PSF), A polyphenylene sulfide (PPS), thermoplastic mold polyphenylene ether (PPE), Polyether sulfone (PES), polyether imide (PEI), polyphenylene sulfone (PPES), polyethylenenaphthalate (PEN), a polyether ether ketone (PEEK), polyolefine system resin, etc. are mentioned. These may be used independently and may use two or more sorts together. In addition, it may replace with the above-mentioned epoxy resin, and these resin may be used.

[0061] (B) next, a conductor — while forming the resin insulating layer between layers which has the Bahia hall on the substrate in which the circuit was formed — this resin insulating-layer top between layers — a conductor — form a circuit. concrete — for example, the following — passing through the process of (i) - (vi) — the resin insulating layer between layers, and a conductor — formation with a circuit is performed. namely, (i) — first — a conductor — the resin layer which forms the non-hardened resin layer which consists of thermosetting resin or resin complex on the substrate in which the circuit was formed, or consists of thermoplastics is formed. The resin layer which is not hardened [above-mentioned] may apply non-hardened resin by the roll coater, a curtain coating machine, etc., may fabricate it, and may carry out thermocompression bonding of the resin film non-hardened (semi-hardening), and may form it. Furthermore, the resin film with which metal layers, such as copper foil, were formed in one side of a non-hardened resin film may be stuck. Moreover, as for the resin layer which consists of thermoplastics, it is desirable to form by carrying out thermocompression bonding of the resin Plastic solid fabricated in the shape of a film.

[0062] In applying the resin which is not hardened [above-mentioned], it performs heat-treatment, after applying resin. Heat curing of the non-hardened resin can be carried out by performing the above-mentioned heat-treatment. In addition, the above-mentioned heat curing may be performed after forming opening for the Bahia halls mentioned later.

[0063] As an example of the thermosetting resin used in formation of such a resin layer, an epoxy resin, phenol resin, polyimide resin, polyester resin, a bismaleimide resin, polyolefine system resin, polyphenylene ether resin, etc. are mentioned, for example.

[0064] As the above-mentioned epoxy resin, a cresol novolak mold epoxy resin, the bisphenol A mold epoxy resin, a bisphenol female mold epoxy resin, a phenol novolak mold epoxy resin, an alkylphenol novolak mold epoxy resin, a biphenol female mold epoxy resin, a naphthalene mold epoxy resin, a dicyclopentadiene mold epoxy resin, the epoxidation object of the condensate of phenols and the aromatic aldehyde which has a phenolic hydroxyl group, triglycidyl isocyanurate, cycloaliphatic epoxy resin, etc. are mentioned, for example. These may be used independently and may be used together two or more sorts. Thereby, it excels in thermal resistance etc.

[0065] As the above-mentioned polyolefine system resin, the copolymer of polyethylene, polystyrene, polypropylene, a polyisobutylene, polybutadiene, polyisoprene, cycloolefin system resin, and these resin etc. is mentioned, for example.
[0066] Moreover, as the above-mentioned thermoplastics, phenoxy resin, polyether sulfone, polysulfone, etc. are mentioned, for example. Moreover, as complex (resin complex) of thermosetting resin and thermoplastics, especially if thermosetting resin and thermoplastics are included, it will not be limited, but as the example, the resin constituent for roughening side formation etc. is mentioned, for example.
[0067] That by which the matter of fusibility was distributed to the roughening liquid which consists of at least one sort chosen from an acid, alkali, and an oxidizer into the heat-resistant-resin matrix which is not hardened [poorly soluble] to the roughening liquid which consists of at least one sort chosen from an acid, alkali, and an oxidizer as the above-mentioned resin constituent for roughening side formation, for example is mentioned. In addition, when the same time amount immersion is carried out, the word of the above "poor solubility" and "fusibility" says relatively what has an early dissolution rate as "fusibility" to the same roughening liquid for convenience, and calls "poor solubility" relatively what has a late dissolution rate to it for convenience.
[0068] In case the above-mentioned roughening liquid is used for the resin insulating layer between layers and a roughening side is formed as the above-mentioned heat-resistant-resin matrix, what can hold the configuration of a roughening side is desirable, for example, thermosetting resin, thermoplastics, these complex, etc. are mentioned. Moreover, you may be a photopolymer. In the process which forms opening for the Bahia halls mentioned later, it is because opening can be formed by the exposure development.
[0069] As the above-mentioned thermosetting resin, an epoxy resin, phenol resin, polyimide resin, polyolefin resin, a fluororesin, etc. are mentioned, for example. Moreover, the resin which made the heat-curing radical acrylic(meta)--ization-react to these thermosetting resin using the resin which gave photosensitivity, i.e., a methacrylic acid, an acrylic acid, etc., may be used. The acrylate (meta) of an epoxy resin is desirable and, specifically, the epoxy resin which has two or more epoxy groups in 1 molecule is more more desirable still.
[0070] As the above-mentioned thermoplastics, phenoxy resin, polyether sulfone, polysulfone, polyphenylene sulfone, polyphenylene sulfide, a polyphenyl ether, polyether imide, etc. are mentioned, for example. These may be used independently and may be used together two or more sorts.
[0071] As matter of the above-mentioned fusibility, an inorganic particle, a resin particle, metal particles, a rubber particle, liquid phase resin, liquid phase rubber, etc. are mentioned, for example. These may be used independently and may be used together two or more sorts.
[0072] As the above-mentioned inorganic particle, the particle which consists of titanium compounds [, such as a silicon compound; titania,], such as magnesium compound; silicas, such as potassium compound; magnesias [, such as lime compound; potassium carbonate,], such as aluminium compound; calcium carbonates, such as an alumina and an aluminum hydroxide, and a calcium hydroxide, a dolomite, basic magnesium carbonate, and talc, and a zeolite, etc. is mentioned, for example. These may be used independently and may be used together two or more sorts. Dissolution removal of the above-mentioned alumina particle can be carried out by fluoric acid, and dissolution removal of the calcium carbonate can be carried out with a hydrochloric acid. Moreover, dissolution removal of a sodium content silica or the dolomite can be carried out in an alkali water solution.
[0073] As the above-mentioned resin particle, what consists of thermosetting resin, thermoplastics, etc. is mentioned, for example. When immersed in the roughening liquid which consists of at least one sort chosen from an acid, alkali, and an oxidizer It will not be limited especially if a dissolution rate is earlier than the above-mentioned heat-resistant-resin matrix. Specifically For example, what consists of amino resin (melamine resin, a urea-resin, guanamine resin, etc.), an epoxy resin, phenol resin, phenoxy resin, polyimide resin, polyphenylene resin, polyolefin resin, a fluororesin, bismaleimide-triazine resin, etc. is mentioned. These may be used independently and may be used together two or more sorts. In addition, the above-mentioned resin particle needs to carry out hardening processing beforehand. It is because the above-mentioned resin particle dissolves in the solvent in which a resin matrix is dissolved, so homogeneity will be mixed and dissolution removal only of the resin particle can be alternatively carried out neither with an acid nor an oxidizer, unless it makes it harden.
[0074] As the above-mentioned metal particles, what consists of gold, silver, copper, tin, zinc, stainless steel, aluminum, nickel, iron, lead, etc. is mentioned, for example. These may be used independently and may be used together two or more sorts. Moreover, the surface may be covered with resin etc. in order that the above-mentioned metal particles may secure insulation.
[0075] (ii) Next, in forming the resin insulating layer between layers using thermosetting resin and resin complex as the ingredient, while performing hardening processing to a non-hardened resin layer, opening for the Bahia halls is formed and it considers as the resin insulating layer between layers. As for the above-mentioned opening for the Bahia halls, forming by the lasing is desirable. The above-mentioned lasing may be performed before the above-mentioned hardening processing, and may be performed after hardening processing. Moreover, when the

resin insulating layer between layers which consists of a photopolymer is formed, opening for the Bahia halls may be prepared by performing exposure and a development. In addition, exposure and a development are performed before the above-mentioned hardening processing in this case.

[0076] Moreover, when forming the resin insulating layer between layers using thermoplastics as the ingredient, opening for the Bahia halls can be formed in the resin layer which consists of thermoplastics by the lasing, and it can consider as the resin insulating layer between layers.

[0077] At this time, carbon dioxide gas laser, excimer laser, UV laser, an YAG laser, etc. are mentioned as laser to be used, for example. These may be properly used in consideration of the configuration of opening for the Bahia halls to form etc.

[0078] When forming the above-mentioned opening for the Bahia halls, much openings for the Bahia halls can be formed at once by irradiating the laser beam by the excimer laser of a hologram method through a mask. Moreover, when opening for the Bahia halls is formed using the carbon dioxide gas laser of a short pulse, there is little resin remainder in opening and the damage to the resin of an opening periphery is small.

[0079] Moreover, when irradiating a laser beam through an optical-system lens and a mask, much openings for the Bahia halls can be formed at once. By minding an optical-system lens and a mask, it is the same reinforcement and is because whenever [illuminating-angle] can irradiate the same laser beam at coincidence at two or more parts.

[0080] (iii) Next, a roughening side is formed in the front face of the resin insulating layer between layers including the wall of opening for the Bahia halls using an acid or an oxidizer if needed. In addition, this roughening side is formed in order to raise the adhesion of the resin insulating layer between layers, and the thin film conductor layer formed on it, and when there is adhesion sufficient between the resin insulating layer between layers and a thin film conductor layer, it is not necessary to form it.

[0081] As the above-mentioned acid, a sulfuric acid, a nitric acid, a hydrochloric acid, a phosphoric acid, formic acid, etc. are mentioned, and permanganates, such as a chromic acid, chromate acid mixture, and sodium permanganate, etc. are mentioned as the above-mentioned oxidizer. Moreover, after forming a roughening side, it is desirable to neutralize the front face of the resin insulating layer between layers using water solutions, neutralization liquid, etc., such as alkali. It is because it can avoid having effect of an acid or an oxidizer on degree process. Moreover, formation of the above-mentioned roughening side may be performed using plasma treatment etc.

[0082] Moreover, the maximum roughness Rmax of the above-mentioned roughening side has desirable 0.1-20 micrometers. if Rmax exceeds 20 micrometers — the roughening side itself — damage and exfoliation — winning popularity — easy — Rmax — less than 0.1 micrometers — a conductor — it is because adhesion with a circuit cannot be acquired enough. especially — a semiadditive process — a conductor — when forming a circuit, the above-mentioned maximum roughness Rmax has desirable 0.1-5 micrometers. While adhesion with a thin film conductor layer is fully securable, it is because removal of a thin film conductor layer is easy.

[0083] (iv) Next, a thin film conductor layer is formed in the front face of the resin insulating layer between layers which prepared opening for the Bahia halls. The above-mentioned thin film conductor layer is formed using approaches, such as nonelectrolytic plating, sputtering, and vacuum evaporationo. In addition, when a roughening side is not formed in the front face of the resin insulating layer between layers, as for the above-mentioned thin film conductor layer, forming by sputtering is desirable. In addition, in forming a thin film conductor layer with nonelectrolytic plating, it gives the catalyst beforehand to the galvanized front face. As the above-mentioned catalyst, a palladium chloride etc. is mentioned, for example.

[0084] Although especially the thickness of the above-mentioned thin film conductor layer is not limited, when this thin film conductor layer is formed with nonelectrolytic plating, 0.6-1.2 micrometers is desirable, and when it forms by sputtering, 0.1-1.0 micrometers is desirable. Moreover, as the quality of the material of the above-mentioned thin film conductor layer, Cu, nickel, P, Pd, Co, W, etc. are mentioned, for example. In these, Cu and nickel are desirable.

[0085] (v) Next, a dry film is used for the part on the above-mentioned thin film conductor layer, plating resist is formed, after that, electrolysis plating is performed by making the above-mentioned thin film conductor layer into a plating bar, and an electrolysis plating layer is formed in the plating-resist agenesis section.

[0086] Moreover, opening for the Bahia halls is filled up with this process with electrolysis plating, and it is good also considering the structure of the Bahia hall as field beer structure, and the Bahia hall which has a hollow is once formed in that top face, this hollow is filled up with a conductive paste after that, and it is good also as field beer structure. Moreover, after forming in a top face the Bahia hall which has a hollow, the hollow is filled up with a resin filler etc., a lid plating layer is further formed on it, and it is good also as a Bahia hall where a top face is flat. The Bahia hall can be formed in right above [of the Bahia hall] by making structure of the Bahia hall into field beer structure.

[0087] (vi) — the conductor which exfoliated plating resist, removed further the thin film conductor layer which existed under plating resist by etching, and became independent — it considers as a circuit. As an etching reagent, persulfate water solutions, such as a sulfuric-acid-hydrogen-peroxide-solution solution and ammonium persulfate, a ferric chloride, a cupric chloride, a hydrochloric acid, etc. are mentioned, for example. Moreover, the mixed solution containing the second copper complex mentioned above as an etching reagent and an organic acid may be used.
[0088] moreover, the thing for which it replaces with the approach of performing removal with plating resist and a thin film conductor layer, and the following approaches are used after forming plating resist on the above-mentioned thin film conductor layer and forming an electrolysis plating layer in the plating-resist agenesis section — a conductor — a circuit may be formed. namely, the conductor which used the dry film for the part on this electrolysis plating layer, formed etching resist, removed an etching-resist agenesis subordinate's electrolysis plating layer and thin film conductor layer by etching after that, and became independent by exfoliating etching resist further after forming an electrolysis plating layer the whole surface on the above-mentioned thin film conductor layer — a circuit may be formed.
[0089] while forming the resin insulating layer between layers which has the Bahia hall by using such an approach — the resin insulating-layer top between layers — a conductor — a circuit can be formed. In addition, in the substrate for IC chip mounting of this invention, although the resin insulating layer between layers forms only one layer, it may carry out laminating formation of the resin insulating layer between layers more than two-layer by repeating this process (B) two or more times depending on the substrate for IC chip mounting to manufacture.
[0090] (C) Next, form a solder resist layer in the outermost layer. After applying a non-hardened solder resist constituent by the roll coater, curtain coater, etc. or specifically sticking by pressure the solder resist constituent fabricated in the shape of a film, a solder resist layer is formed by performing hardening processing.
[0091] The above-mentioned solder resist layer is [0092] which can be formed using the solder resist constituent containing for example, polyphenylene ether resin, polyolefin resin, a fluororesin, thermoplastic elastomer, an epoxy resin, polyimide resin, etc. moreover, as solder resist constituents other than the above For example, the acrylate (meta) of a novolak mold epoxy resin, an imidazole curing agent, 2 functionality (meta) acrylic ester monomer, the polymer of with a molecular weight of about 500 to 5000 acrylic ester (meta), The fluid of the shape of a paste containing photosensitive monomers, such as thermosetting resin which consists of a bisphenol mold epoxy resin etc., and a multiple-valued acrylic monomer, a glycol ether system solvent, etc. is mentioned, and, as for the viscosity, it is desirable to be adjusted to 1 - 10 Pa-s at 25 degrees C. Moreover, as for the above-mentioned solder resist constituent, the elastomer and the inorganic filler may be blended. Moreover, a commercial solder resist constituent may be used as a solder resist constituent.
[0093] Moreover, opening is formed in the above-mentioned solder resist layer by the lasing or the exposure development if needed. Under the present circumstances, the same thing as the laser used in case opening for the Bahia halls mentioned above is formed as laser to be used etc. is mentioned.
[0094] next, the conductor exposed to the base of the above-mentioned opening — a metal layer is formed on the surface of a circuit if needed. In addition, the metal layer formed in opening at this process may play a role of a solder pad, when the solder resist layer which has this opening constitutes the outermost layer of the substrate for IC chip mounting. the above-mentioned metal layer — corrosion-resistant metals, such as nickel, palladium, gold, silver, and platinum, — the above — a conductor — it can form by covering a circuit front face. Specifically, it is desirable to form with metals, such as nickel-gold, nickel-silver, nickel-palladium, and nickel-palladium-gold. Moreover, although the above-mentioned solder pad can be formed using approaches, such as plating, vacuum evaporationo, and electrodeposition, in these, the point of excelling in the homogeneity of an enveloping layer to its plating is desirable. Moreover, the mark for alignment used at the process mentioned later in the case of lamination with an optical wiring layer may be formed in the solder resist layer formed at this process. Such (A) A package substrate is producible by passing through the process of - (C).
[0095] Next, the production approach of an optical wiring layer is explained. Production of an optical wiring layer can be performed by passing through the process of for example, following (a) - (c).
(a) first — both sides or one side of a substrate — nonelectrolytic plating processing etc. — a conductor — form a circuit. performing etching processing, after forming a solid conductor layer by nonelectrolytic plating processing etc. on a substrate and specifically forming a resist on this conductor layer — a substrate top — a conductor — a circuit is formed. moreover, the thing for which plating resist is formed on a substrate and plating processing and exfoliation of plating resist are performed after that — a substrate top — a conductor — a circuit may be formed.
[0096] moreover, the conductor whose substrate was pinched at this process — the through hole which connects between circuits may be formed. forming a conductor layer also in the wall surface of a through tube,

in case the through tube is formed in the substrate by drilling, the lasing, etc. and a solid conductor layer is formed, and performing etching processing after that beforehand, before formation of a through hole forms a solid conductor layer for example, by nonelectrolytic plating processing etc. — a conductor — a through hole may be formed while forming a circuit. moreover, the thing for which nonelectrolytic plating processing etc. is performed to the wall surface of this through tube, and etching processing is further performed to a conductor layer after forming a through tube in the substrate with which the solid conductor layer was formed beforehand — a conductor — a circuit and a through hole may be formed.

[0097] moreover, the thing which plating resist is formed in a part of front face of a substrate, and a conductor layer is formed in the wall surface and the plating-resist agenesis section of a through tube after that, and is further exfoliated in plating resist after forming a through tube in a substrate — a conductor — a circuit and a through hole may be formed. Moreover, before forming a conductor layer after forming a through tube in forming a through tube in a substrate by these approaches, it is desirable to perform DESUMIA processing to this through tube. For example, drug solution processing, dry processing using the plasma, etc. are mentioned, using oxidizers, such as permanganic acid and a chromic acid, as the above-mentioned DESUMIA processing.

[0098] The same thing as the substrate used as a substrate used here, for example in case a package substrate is formed etc. is mentioned. Moreover, also in the process which produces this optical wiring layer, after forming the above-mentioned through hole, it is desirable for it to be filled up with a resin filler and to form a resin filler layer in this through hole. In addition, restoration of a resin filler can lay on a substrate the mask with which opening was formed in the part equivalent to a through hole, and can be performed using a squeegee. Moreover, also in this process, before being filled up with a resin filler in a through hole, it is desirable to form a roughening side in the wall surface of a through hole. Thereby, it is because the adhesion of a through hole and a resin filler layer improves more. The same thing as the resin filler used as the above-mentioned resin filler, for example when forming a package substrate etc. can be used.

[0099] moreover, this conductor — in a circuit formation process, after forming a resin filler layer in a through hole, a wrap lid plating layer may be formed for the exposure from the through hole of this resin filler layer. It is because it becomes possible to form a solder pad by forming a lid plating layer not only the land top of a through hole but on a lid plating layer, so the degree of freedom of a design improves more.

[0100] After the above-mentioned lid plating layer forms a conductor layer in the front face of the substrate containing the exposure of for example, a resin filler layer and forms etching resist in a lid plating stratification part, it performs etching processing, or forms plating resist in the lid plating layer agenesis part beforehand, and can form it by performing plating processing and removal of plating resist.

[0101] therefore, the thing processed in the following procedure in this process when forming a lid plating layer on a through hole — a conductor — formation of a circuit and a through hole and formation of a lid plating layer can be performed to coincidence. That is, first, after forming a through tube in a substrate, a conductor layer is formed in the front face of the substrate containing the wall surface of this through tube, and, subsequently to the wall surface, it is filled up with a resin filler in the through tube in which the conductor layer was formed. furthermore, the conductor after carrying out laminating formation of the conductor layer by plating processing etc. on the conductor layer formed in the exposure and substrate front face of a resin filler — carrying out etching removal of the conductor layer of the circuit agenesis section and the through hole agenesis section — a conductor — formation of a circuit and a through hole and formation of a lid plating layer can be performed to coincidence.

[0102] (b) next, a conductor — the conductor on the substrate in which the circuit was formed — form an adhesives layer in a part of circuit agenesis section [at least]. in addition, this specification — setting — the land part of a through hole — a conductor — it shall contain in a circuit therefore, the land part of a through hole — a conductor — it is not equivalent to the circuit agenesis section. the near conductor stuck with a package substrate at a back process in this process — an adhesives layer is formed in all or a part of circuit agenesis sections. What is necessary is just to apply the above-mentioned adhesives layer so that sufficient adhesive property with a package substrate may be acquired. Therefore, it is ** [it may form an adhesives layer in the part which forms a through tube at the process of (c) mentioned later].

[0103] As the above-mentioned adhesives, thermosetting resin, thermoplastics, a photopolymer, the resin with which a part of heat-curing radical was sensitization-ized, the thing which consists of these complex can be used, for example. As an example, an epoxy resin, phenol resin, polyimide resin, BT resin, etc. are mentioned, for example. Moreover, the adhesives fabricated in the shape of a sheet may be used beforehand, and prepreg may be used.

[0104] (c) Form a through tube in some substrates which formed the adhesives layer next. In the through tube formed here, an optical element will be arranged in a back process. For example, router processing etc. can perform formation of the above-mentioned through tube. Moreover, although especially the formation location of

the above-mentioned through tube is not limited, it is usually formed in the center of a substrate.
[0105] Moreover, in this process, after forming a through tube, in order to remove the weld flash which exists in a through tube wall surface, drug solution processing, polish processing, etc. may be performed. The above-mentioned drug solution processing can be performed using the oxidizer which consists of water solutions, such as a chromic acid and a permanganate. Such (a) An optical wiring layer is producible by passing through the process of - (c).
[0106] Next, after sticking the optical wiring layer produced through the process of the package substrate produced through the process of - (C), and (above-mentioned A) above-mentioned (a) - (c) through the adhesives layer which this optical wiring layer has, how to use as the substrate for IC chip mounting is explained.

[0107] Lamination of a package substrate and an optical wiring layer can be performed using for example, a pin lamination method, a mass lamination method, etc. After performing both alignment, specifically, a package substrate and an optical wiring layer are stuck by carrying out a temperature up to the temperature (usually about 60-200 degrees C) which an adhesives layer softens, and subsequently pressing by the pressure of 1 - 10MPa extent. Then, it considers as the substrate for IC chip mounting through the process of following the (1) - (3).
[0108] (1) the conductor of the above-mentioned optical element after attaching an optical element in the front face of the package substrate first exposed from the through tube formed in the above-mentioned optical wiring layer, and the above-mentioned package substrate -- connect a circuit electrically. Installation of the above-mentioned optical element can be performed by for example, the eutectic joining-together method, the solder joining-together method, a resin bond method, etc. Moreover, an optical element may be attached using a silver paste metallurgy paste. By the describing [above] resin bond method, thermosetting resin, such as epoxy system resin and polyimide system resin, is used as base resin, the paste which contains a curing agent, a filler, a solvent, etc. in addition to these resinous principles is applied on a package substrate, and subsequently to a paste top, after laying an optical element, an optical element is attached by carrying out heat hardening of this paste. In addition, spreading of the above-mentioned paste can be performed with for example, the dispensing method, the **********ing method, screen printing, etc. Moreover, in using a silver paste, a silver paste is applied on a package substrate, and after laying an optical element, subsequently to a paste top, it attaches an optical element by calcinating this ****-strike.
[0109] As an approach of connecting electrically the above-mentioned optical element and the metal layer of the above-mentioned package substrate, it is desirable to use wirebonding. It is because it is economically advantageous while this has the large degree of freedom of the design at the time of attaching an optical element. As the above-mentioned wirebonding, a well-known approach, i.e., the nail-head-bonding method and the wedge bonding method, can be used conventionally. In addition, tape automated bonding, flip chip bonding, etc. may perform mounting of an optical element.
[0110] (2) Next, in the through tube formed in the above-mentioned optical wiring layer, it is filled up with a resin constituent and form a resin packed bed. As mentioned above, since the resin packed bed is formed from two-layer [of a lower layer resin packed bed and the upper resin packed bed], with the substrate for IC chip mounting of this invention, a resin constituent is filled up with this process in 2 steps.
[0111] It is not limited especially as an approach filled up with a resin constituent, for example, approaches, such as printing and potting, can be used. Moreover, it may be filled up with what was made into the shape of a tablet using a plunger. Moreover, after being filled up with a resin packed bed, hardening processing etc. is performed if needed. Moreover, after the above-mentioned hardening processing is filled up with the resin constituent used as a lower layer resin packed bed, it is performed once, after it is filled up with the resin constituent used as the upper resin packed bed, it may be performed again, and after it is filled up with both the resin constituents used as the resin constituent used as a lower layer resin packed bed, and the upper resin packed bed, it may be performed to coincidence. According to a resin constituent, it should just determine suitably which approach is chosen. When hardening conditions with the resin constituent used as the resin constituent which serves as a lower layer resin packed bed especially, and the upper resin packed bed differ, after being filled up with the resin constituent used as a lower layer resin packed bed, it is desirable to perform once hardening processing and to perform restoration and hardening processing of the resin constituent used as the upper resin packed bed after that. Moreover, when this approach is used, it is not mixed with the resin constituent used as the resin constituent used as a lower layer resin packed bed, and the upper resin packed bed by that interface.
[0112] Furthermore, it is desirable to perform polish processing to the exposure of the resin constituent exposed from the through tube at this process, and to make that exposure flat. By making an exposure flat, it is because a possibility that transmission of communication link light may be checked decreases more. Polish by buffing, a sandpaper, etc., mirror polishing, clean polish, wrapping, etc. can perform the above-mentioned polish processing.

Moreover, chemical polishing using an acid, an oxidizer, a drug solution, etc. may be performed. Moreover, two or more sorts of polish processings may be performed combining these approaches.
[0113] Moreover, after forming the above-mentioned resin packed bed, the through hole which penetrates the above-mentioned package substrate and the above-mentioned optical wiring layer may be formed if needed. A thin film conductor layer is formed in the exposure of the package substrate which specifically forms first the through tube for through holes which penetrates the above-mentioned package substrate and the above-mentioned optical wiring layer by drilling, the lasing, etc., next contains the wall surface of this through tube for through holes, and the exposure of an optical wiring layer by nonelectrolytic plating, sputtering, etc. Furthermore, after forming plating resist on the substrate with which the thin film conductor layer was formed in the front face, the through hole which penetrates the above-mentioned package substrate and the above-mentioned optical wiring layer is formed by forming an electrolysis plating layer in this plating-resist agenesis section, and removing the thin film conductor layer under the above-mentioned plating resist and this plating resist after that.

[0114] As the quality of the material of the above-mentioned thin film conductor layer, copper, nickel, tin, zinc, cobalt, a thallium, lead, etc. are mentioned, for example. In these, what consists of the copper from a point, copper, and nickel which are excellent in an electrical property, economical efficiency, etc. is desirable. Moreover, as thickness of the above-mentioned thin film conductor layer, when forming a thin film conductor layer with nonelectrolytic plating, 0.3-2.0 micrometers is desirable and 0.6-1.2 micrometers is more desirable. Moreover, when forming by sputtering, 0.1-1.0 micrometers is desirable.
[0115] As the above-mentioned electrolysis plating, copper plating is desirable and 5-20 micrometers is desirable as the thickness. Moreover, what is necessary is just to perform removal of the above-mentioned thin film conductor layer using etching reagents, such as mixed liquor of a sulfuric acid and a hydrogen peroxide, sodium persulfate, ammonium persulfate, a ferric chloride, and a cupric chloride, that what is necessary is just to perform removal of the above-mentioned plating resist for example, using an alkali water solution etc. moreover, the above -- a conductor -- after forming a circuit, the catalyst on the resin insulating layer between layers may be removed using an acid or an oxidizer if needed. It is because the fall of an electrical property can be prevented.
[0116] Moreover, after forming a through hole, it is desirable to be filled up with a resin filler in this through hole. As the above-mentioned resin filler, the same thing as the resin filler used for the restoration in a through hole etc. can be used, for example in production of a package substrate.
[0117] Moreover, when it is filled up with a resin filler and a resin filler layer is formed in a through hole, a wrap lid plating layer may be formed for the surface section of a resin filler layer by performing nonelectrolytic plating etc. if needed. It is because it becomes possible to form a solder pad by forming a lid plating layer not only the land top of a through hole but on a lid plating layer, so the degree of freedom of a design improves more.
[0118] Moreover, after replacing with the approach of forming an electrolysis plating layer after forming plating resist which was mentioned above and forming an electrolysis plating layer the whole surface on a thin film conductor layer, etching resist and a solder plating layer may be formed on an electrolysis plating layer, and you may form the through hole further penetrated in the above-mentioned optical wiring layer and the above-mentioned package substrate using the approach of performing etching processing. In addition, after forming a through hole, it is desirable to be filled up with a resin filler in this through hole, and the same thing as the resin filler with which it was filled up in the through hole formed as a resin filler at the package substrate or the optical wiring layer etc. is mentioned.
[0119] In addition, after formation of the through hole explained here performs formation of mounting of an optical element, a lower layer resin packed bed, and the upper resin packed bed, it is not necessarily necessary to perform it, before it mounts an optical element, it may be performed, and before forming a lower layer resin packed bed and the upper resin packed bed, it may be performed.
[0120] (3) Next, form a solder resist layer in the exposure of the above-mentioned package substrate, or the exposure of the above-mentioned optical wiring layer. After applying a non-hardened solder resist constituent by the roll coater, curtain coater, etc. or specifically sticking by pressure the solder resist constituent fabricated in the shape of a film, a solder resist layer is formed by performing hardening processing. The same thing as the solder resist constituent used as the above-mentioned solder resist constituent, for example when producing a package substrate etc. can be used.
[0121] In addition, in this process, it is not necessary to form a solder resist layer on the resin packed bed formed at the process of the above (2). Moreover, when the through hole which carries out the through tube of a package substrate and the optical wiring layer in the process of the above (2) is not formed, in this process, it is not necessary to form a solder resist layer in the exposure of a package substrate. Before performing this process, it is because the solder resist layer is already formed in all the exposures of a package substrate.

[0122] Moreover, opening for solder bump formation is formed in the above-mentioned solder resist layer by the lasing or the exposure development if needed. Under the present circumstances, the same thing as the laser used in case opening for the Bahia halls mentioned above is formed as laser to be used etc. is mentioned.
[0123] In addition, after formation of the solder resist layer explained here performs formation (process of the above (2)) of mounting (process of the above (1)) of an optical element, a lower layer resin packed bed, and the upper resin packed bed, it is not necessarily necessary to perform it, before it mounts an optical element, it may be performed, and before forming a lower layer resin packed bed and the upper resin packed bed, it may be performed. In addition, when you form a solder resist layer before performing the process of the above (1), and the process of (2), since an optical element mounts, it supposes that the front face of the package substrate exposed to the base of the through tube formed in the optical wiring layer is not contained, and suppose at the exposure of the above-mentioned optical wiring layer that the wall surface of the through tube formed in this optical wiring layer is not contained at the exposure of the above-mentioned package substrate. Moreover, as mentioned above, when forming the through hole which penetrates a package substrate and an optical wiring layer, formation of the above-mentioned solder resist layer is performed after forming a through hole.
[0124] next, the conductor exposed to the base of the above-mentioned opening for solder bump formation — a metal layer is formed on the surface of a circuit if needed. the above-mentioned metal layer — corrosion-resistant metals, such as nickel, palladium, gold, silver, and platinum, — the above — a conductor — it can form by covering a circuit front face. Specifically, it is desirable to form with metals, such as nickel-gold, nickel-silver, nickel-palladium, and nickel-palladium-gold. Moreover, although the above-mentioned metal layer can be formed using approaches, such as plating, vacuum evaporationo, and electrodeposition, in these, the point of excelling in the homogeneity of an enveloping layer to its plating is desirable. In addition, in case this metal layer forms a solder bump etc. at a back process, it will play a role of a solder pad.
[0125] Furthermore, after filling up the above-mentioned opening for solder bump formation with soldering paste through the mask with which opening was formed in the part equivalent to the above-mentioned opening for solder bump formation if needed, the solder bump for flip chips and the solder bump for BGA (Ball GridArray) are formed by carrying out a reflow. The substrate for IC chip mounting can be manufactured by passing through such a series of processes.
[0126] IC chip will usually be mounted in the substrate for IC chip mounting of this invention manufactured by such approach after manufacture. When for example, the above-mentioned solder bump for a PURIPPU chip is formed, mounting of the above-mentioned IC chip performs PURIPPU chip mounting of IC chip through this solder bump, and is performed after that if needed by closing between IC chip and the substrates for IC chip mounting by resin. Moreover, wirebonding may perform mounting of the above-mentioned IC chip. Of course, it is not necessary to form the solder bump for a PURIPPU chip in this case.
[0127] In addition, although the solder bump for a PURIPPU chip for mounting IC chip and the solder bump for BGA for connecting the substrate for IC chip mounting to other substrates (mother board etc.) are formed at the same process in the approach of manufacturing the substrate for IC chip mounting of this invention mentioned above After not forming two kinds of this solder bump at the same process, for example, forming only the solder bump for flip chips first and mounting IC chip through this solder bump, the solder bump for BGA may be formed using soldering paste or a solder ball.
[0128]
Example] Hereafter, this invention is further explained to a detail.
Example 1)
A. The production bisphenol A mold epoxy resin (weight-per-epoxy-equivalent 469, Epicoat 1001 by oil-ized shell epoxy company) 30 weight section of the resin film for the resin insulating layers between the (production 1) layers, [of a package substrate] The cresol novolak mold epoxy resin (weight-per-epoxy-equivalent 215, Epiclon N-673 by Dainippon Ink & Chemicals, Inc.) 40 weight section, The triazine structure content phenol novolak resin (phenol nature hydroxyl equivalent 120, Dainippon Ink & Chemicals, Inc. make FENO light KA-7052) 30 weight section The ethyl diethylene glycol acetate 20 weight section, The heating dissolution is carried out stirring in the solvent naphtha 20 weight section. There The end epoxidation polybutadiene rubber (Nagase Brothers formation DENAREKKUSU R-45 by industrial company EPT) 15 weight section, and the 2-phenyl -4, the 5-screw (hydroxymethyl) imidazole grinding article 1.5 weight section, The pulverizing silica 2 weight section and the silicon system defoaming agent 0.5 weight section were added, and the epoxy resin constituent was prepared. After applying using a roll coater so that the thickness after drying the obtained epoxy resin constituent on a PET film with a thickness of 38 micrometers may be set to 50 micrometers, the resin film for the resin insulating layers between layers was produced by making it dry for 10 minutes at 80-120 degrees C.
[0129] The mean particle diameter by which coating of the silane coupling agent was carried out to the reparation bisphenol female mold epoxy monomer (oil-ized shell company make, molecular weight : 310 YL983U)

100 weight section of a resin filler and a front face (b) By 1.6 micrometers the diameter of grain of maximum size — SiO2 spherical particle (the Adtec Corp. make —) 15 micrometers or less CRS The viscosity prepared the resin filler of 30 - 60 Pa-s at 23**1 degree C by carrying out stirring mixing of the 1101-CE72 weight section and the leveling agent (Sannopuko PERENORU S4) 1.5 weight section for a container. In addition, the imidazole curing agent (Shikoku formation shrine make, 2E4 MZ-CN) 6.5 weight section was used as a curing agent.
[0130] (c) Double-sided copper clad laminate which 18-micrometer copper foil 28 laminates to both sides of the insulating substrate 21 which consists of the glass epoxy resin with a manufacture (1) thickness of 0.8mm or BT (bismaleimide triazine) resin of a package substrate was used as the start ingredient (refer to drawing 3 (a)). first, the thing which drill drilling of this copper clad laminate is carried out, and nonelectrolytic plating processing is performed, and is etched in the shape of a pattern — both sides of a substrate — a lower layer — a conductor — the circuit 24 and the through hole 29 were formed (refer to drawing 3 (b)).
[0131] (2) a lower layer — a conductor — washing in cold water the substrate 21 in which the circuit 24 was formed, and, after drying Melanism processing the water solution containing NaOH (10g/(l.)), NaClO2 (40 g/l), and Na3PO4 (6 g/l) — melanism — it considers as a bath (oxidation bath) — and the reduction processing which makes a reduction bath NaOH (10 g/l) and the water solution containing NaBH4 (6 g/l) — carrying out — a lower layer — a conductor — the roughening side (not shown) was formed in the front face of a circuit 24.
[0132] (3) next, the following approach after preparing the resin filler indicated above (b) — after preparation — less than 24 hours — the conductor of one side of the inside of a through hole 29, and a substrate 21 — the circuit agenesis section and a lower layer — a conductor — the layer of resin filler 30' was formed in the rim section of a circuit 24. That is, after pushing in a resin filler in a through hole using a squeegee, it was made to dry on 100 degrees C and the conditions for 20 minutes first. next, a conductor — the conductor with which the part equivalent to the circuit agenesis section lays on a substrate the mask which carried out opening, and serves as a crevice using the squeegee — the circuit agenesis section was also filled up with the resin filler, and the layer of resin filler 30' was formed by making it dry on 100 degrees C and the conditions for 20 minutes (refer to drawing 3 R> 3 (c)).
[0133] (4) the belt sander [one side / which finished processing of the above (3) / of a substrate] polish using the belt abrasive paper (Sankyo Rikagaku make) of **600 — a conductor — it ground so that resin filler 30' might remain neither in the front face of a circuit 24, nor the land front face of a through hole 29, and subsequently buffing for removing the blemish by the above-mentioned belt sander polish was performed. Such a series of processings were similarly performed about the field of another side of a substrate. Subsequently, by 100 degrees C, it performed at 150 degrees C for 1 hour for 3 hours, 120 degrees C performed heat-treatment of 7 hours at 180 degrees C for 1 hour, and the resin filler layer 30 was formed.
[0134] Flattening of the front face of a circuit 24 is carried out. thus, a through hole 29 and a conductor — the surface section of the resin filler layer 30 formed in the circuit agenesis section, and a conductor — the resin filler layer 30 and a conductor — the insulating substrate which the side face of a circuit 24 stuck firmly through the roughening side (not shown), and the internal surface and the resin filler layer 30 of a through hole 29 stuck firmly through the roughening side (not shown) was obtained (refer to drawing 3 (d)). this process — the front face of the resin filler layer 30, and a conductor — the front face of a circuit 24 turns into the same flat surface.

[0135] (5) software etching after rinsing and carrying out acid cleaning of the above-mentioned substrate — carrying out — subsequently — an etching reagent — both sides of a substrate — a spray — spraying — a conductor — etching the front face of a circuit 24, and the land front face of a through hole 29 — a conductor — the roughening side (not shown) was formed in all the front faces of a circuit 24. As an etching reagent, the etching reagent (the product made from MEKKU, MEKKU dirty bond) containing the imidazole copper (II) complex 10 weight section, the glycolic-acid 7 weight section, and the potassium chloride 5 weight section was used.
[0136] (6) Next, by 0.5MPa, it laminated vaccum pressure arrival, the resin film for the resin insulating layers between layers produced above (a) was stuck, carrying out a temperature up to the temperature of 50-150 degrees C, and resin film layer 22alpha was formed (refer to drawing 3 (e)).
[0137] (7) Next, mind the mask with which the through tube with a thickness of 1.2mm was formed on resin film layer 22alpha. In CO2 gas laser with a wavelength of 10.4 micrometers, the beam diameter of 4.0mm, the Top Hat mode, On 8.0 microseconds of pulse width, the path of 1.0mm of the through tube of a mask, and the conditions of one shot, the opening 26 for the Bahia halls with a diameter of 80 micrometers was formed in resin film layer 22alpha, and it considered as the resin insulating layer 22 between layers (refer to drawing 4 R> 4 (a)).
[0138] (8) The roughening side (not shown) was formed in the front face of the resin insulating layer 22 between layers containing the internal surface of the opening 26 for the Bahia halls by immersing the substrate in which the opening 26 for the Bahia halls was formed, for 10 minutes in the 80-degree C solution containing 60g [/l.] permanganic acid, and carrying out dissolution removal of the epoxy resin particle which exists in the front face

of the resin insulating layer 22 between layers.
[0139] (9) Next, the substrate which finished the above-mentioned processing was washed in cold water after being immersed in the neutralization solution (product made from SHIPUREI). Furthermore, the catalyst nucleus was made for the front face of this substrate that carried out the surface roughening process (a roughening depth of 3 micrometers) to adhere to the front face (for the internal surface of the opening 26 for the Bahia halls to be included) of the resin insulating layer 22 between layers by giving a palladium catalyst (not shown). That is, the above-mentioned substrate was immersed into the catalytic liquid containing a palladium chloride (PdCl2) and a stannous chloride (SnCl2), and the catalyst was given by depositing a palladium metal.
[0140] (10) Next, into the non-electrolytic copper plating liquid of the following presentations, the substrate was immersed and the non-electrolytic copper plating film (thin film conductor layer) 32 with a thickness of 0.6-3.0 micrometers was formed on the front face (the internal surface of the opening 26 for the Bahia halls is included) of the resin insulating layer 22 between layers (refer to drawing 4 (b)).
[Nonelectrolytic plating liquid]
NiSO4 0.003 mol/l tartaric acid 0.200 mol/l copper sulfate 0.030 mol/lHCHO 0.050 mol/lNaOH 0.100 mol/lalpha and alpha'-bipyridyl 100 mg/l polyethylene glycol (PEG) 0.10 g/l [nonelectrolytic plating conditions]
It is 40 minutes [0141] by whenever [34-degree C solution temperature]. (11) Next, plating resist 23 was formed by sticking a commercial photosensitive dry film on the substrate with which the non-electrolytic copper plating film 32 was formed, laying a mask, exposing by 100 mJ/cm2, and carrying out a development in a sodium-carbonate water solution 0.8% (refer to drawing 4 (c)).
[0142] (12) Subsequently, 50-degree C water washed the substrate and it degreased, with 25-degree C water, after washing with the sulfuric acid further after rinsing, electrolysis plating was performed on condition that the following, and the electrolytic copper plating film 33 was formed in the plating-resist 23 agenesis section (refer to drawing 4 R> 4 (d)).
[Electrolysis plating liquid]
Sulfuric acid 2.24 mol/l copper sulfate 0.26 mol/l additive 19.5 ml/l (made in ATOTEKKU Japan, KAPARASHIDO GL)
[Electrolysis plating conditions]
Current density 1 A/dm 2 hours 65 Part temperature 22**2 ** [0143] (13) — the nonelectrolytic plating film under the plating resist 23 after carrying out exfoliation removal of the plating resist 23 by KOH 5% further — the mixed liquor of a sulfuric acid and a hydrogen peroxide — etching processing — carrying out — dissolution removal — carrying out — the upper layer — a conductor — it considered as the circuit 25 (the Bahia hall 27 is included) (refer to drawing 5 (a)).
[0144] (14) next, the upper layer — a conductor — the substrate in which the circuit 25 grade was formed — an etching reagent — being immersed — the upper layer — a conductor — the roughening side (not shown) was formed in the front face of a circuit 25 (the Bahia hall 27 is included). In addition, as an etching reagent, the product made from MEKKU and MEKKU dirty bond were used.
[0145] (15) Next, made it dissolve so that it may become 60% of the weight of concentration to diethylene-glycol wood ether (DMDG). The oligomer (molecular weight: 4000) 46.67 weight section of the photosensitive grant which acrylic-ized 50% of epoxy groups of a cresol novolak mold epoxy resin (Nippon Kayaku Co., Ltd. make), 80% of the weight of the bisphenol A mold epoxy resin (oil-ized shell company make —) dissolved in the methyl ethyl ketone trade name: — the Epicoat 1001 15.0 weight section and an imidazole curing agent (Shikoku — formation — shrine make —) trade name: — 2 organic-functions acrylic monomer (the Nippon Kayaku Co., Ltd. make —) which are the 2E4 MZ-CN1.6 weight section and a photosensitive monomer trade name: — the R604 4.5 weight section — the same — a multiple-valued acrylic monomer (the Kyoei Kagaku K.K. make —) trade name: — the DPE6A1.5 weight section and a dispersed system defoaming agent (the Sannopuko make —) Stir the S-65 0.71 weight section for a container, mix, and a mixed constituent is prepared. The solder resist constituent which adjusted viscosity to 2.0 Pa-s at 25 degrees C was obtained by adding the benzophenone (Kanto chemistry company make) 2.0 weight section and the Michler's-ketone (Kanto chemistry company make) 0.2 weight section as a photosensitizer as a photopolymerization initiator to this mixed constituent. Moreover, in the case of 60rpm (min-1), in the case of rotor No.4 and 6rpm (min-1), measurement of viscosity was based on rotor No.3 by the Brookfield viscometer (the Tokyo Keiki Co., Ltd. make, DVL-B mold). In addition, a commercial solder resist constituent can also be used as a solder resist constituent.
[0146] (16) next, the upper layer — a conductor — the above-mentioned solder resist constituent was applied, for 20 minutes was performed at 70 degrees C, desiccation processing was performed to both sides of the substrate in which the circuit 25 grade was formed, the condition for 30 minutes at 70 degrees C, and layer 34alpha of a solder REJISU constituent was formed in them (refer to drawing 5 (b)). Subsequently, the photo mask with a thickness of 5mm with which the pattern of opening was drawn was stuck to layer 34alpha of a

solder resist constituent, it exposed by the ultraviolet rays of 1000 mJ/cm2, the development was carried out with the DMTG solution, and opening 31 was formed. And further, it carried out at 120 degrees C for 1 hour for 1 hour, heat-treated [80 degrees C / 1 hour and 100 degrees C] on the conditions of 3 hours by 150 degrees C, respectively, layer 34alpha of a solder resist constituent was stiffened, and the solder resist layer 34 which has opening 31 was formed (refer to drawing 5 (c)).

[0147] (17) Next, the substrate in which the solder resist layer 34 was formed was immersed in the non-electrolyzed nickel-plating liquid of pH=4.5 containing a nickel chloride (2.3x10-1 mol/l), sodium hypophosphite (2.8x10-1 mol/l), and a sodium citrate (1.6x10-1 mol/l) for 20 minutes, and the nickel-plating layer was formed in a part of opening 31. Furthermore, the substrate was immersed in the non-electrolyzed gilding liquid containing a gold cyanide potassium (7.6x10-3 mol/l), an ammonium chloride (1.9x10-1 mol/l), a sodium citrate (1.2x10-1 mol/l), and sodium hypophosphite (1.7x10-1 mol/l) for 7.5 minutes on 80-degree C conditions, the gilding layer was formed on the nickel-plating layer, and it considered as the package substrate (refer to drawing 5 (d)). In addition, all over drawing, two-layer [of a nickel-plating layer and a gilding layer] is doubled, and it is indicated as the metal layer 36.

[0148] B. It carried out using the same approach as the process of (b) of production of the preparation above-mentioned package substrate of (Production a) resin filler of an optical wiring layer.

[0149] (b) Double-sided copper clad laminate which 18-micrometer copper foil 8 laminates to both sides of the insulating substrate 1 which consists of the glass epoxy resin with a manufacture (1) thickness of 0.8mm or BT (bismaleimide triazine) resin of an optical wiring layer was used as the start ingredient (refer to drawing 6 (a)). First, the conductor layer 12 was formed in that front face (the wall surface of a through tube is included) by carrying out drill drilling of this copper clad laminate, and performing nonelectrolytic plating processing (refer to drawing 6 (b)).

[0150] (2) Next, after washing in cold water the substrate 1 in which the conductor layer 12 was formed and drying, Melanism processing the water solution containing NaOH (10g/(l.)), NaClO2 (40 g/l), and Na3PO4 (6 g/l) -- melanism -- it considers as a bath (oxidation bath) -- And reduction processing which makes a reduction bath NaOH (10 g/l) and the water solution containing NaBH4 (6 g/l) was performed, and the roughening side (not shown) was formed in the front face of a conductor layer 12.

[0151] (3) Next, after preparing the resin filler indicated above (a), the layer of resin filler 10' was formed in the through tube which formed the conductor layer 12 in the wall surface within 24 hours after preparation by the following approach. That is, after pushing in a resin filler in a through tube using a squeegee, it was made to dry on 100 degrees C and the conditions for 20 minutes (refer to drawing 6 (c)).

[0152] (4) By belt sander polish using the belt abrasive paper (Sankyo Rikagaku make) of **600, one side of a substrate which finished processing of the above (3) was ground so that the exposure of the layer of resin filler 10' and the front face of a conductor layer 12 might become flat, and subsequently buffing for removing the blemish by the above-mentioned belt sander polish was performed. Such a series of polishes were similarly performed about the field of another side of a substrate. Subsequently, by 100 degrees C, it performed at 150 degrees C for 1 hour for 3 hours, 120 degrees C performed heat-treatment of 7 hours at 180 degrees C for 1 hour, and the resin filler layer 10 was formed (refer to drawing 6 (d)).

[0153] (5) Next, the conductor layer 14 was formed by performing nonelectrolytic plating processing to one side of the substrate in which the conductor layer 12 was formed (refer to drawing 6 (e)). In addition, the conductor layer 14 was beforehand formed in the field of the side which gives the palladium catalyst and does not form a conductor layer 14 by forming plating resist in the field which forms a conductor layer 14 at one side of a substrate.

[0154] (6) the conductor of the substrate in which the conductor layer 12 and the conductor layer 14 were formed -- by performing etching processing, after forming etching resist (not shown) in the part equivalent to the circuit (land part of through hole is included) formation section the through hole 6 where the resin filler layer 10 was formed in the interior, and the lid plating layer 16 was formed in the upper part, and a conductor -- the circuit (not shown) was formed (refer to drawing 6 (f)).

[0155] In addition, formation of etching resist stuck the commercial photosensitive dry film, laid the mask, exposed it by 100 mJ/cm2, and was performed by carrying out a development in a sodium-carbonate water solution 0.8%. Moreover, etching processing was performed using the mixed liquor of a sulfuric acid and a hydrogen peroxide.

[0156] (7) next, the conductor of one side of a substrate -- the adhesives layer (not shown) was formed by applying epoxy resin adhesive to the circuit agenesis section.

(8) Further, the through tube 9 was formed in the center section of a substrate by router processing, and it considered as the optical wiring layer (refer to drawing 6 (g)).

[0157] C. The laminating press by the production (1) mass lamination method of the substrate for IC chip

mounting was performed, and the substrate which stuck the package substrate produced by Above A and the optical wiring layer produced by Above B through the adhesives layer formed in the above-mentioned optical wiring layer was obtained (refer to drawing 7 (a)). That is, after performing both alignment, a temperature up is carried out to 150 degrees C, and the package substrate and the optical wiring layer were stuck by pressing in a pan by the pressure of 5MPa(s).

[0158] (2) Next, the photo detector 38 and the light emitting device 39 were attached in the front face of the package substrate exposed from the through tube 9 formed in the optical wiring layer using the silver paste so that light sensing portion 38a and light-emitting part 39a might be up exposed, respectively. In addition, as a photo detector 38, what consists of InGaAsP was used as a light emitting device 39 using what consists of InGaAs.

[0159] (3) Next, the metal layer 36 of the front face of the package substrate exposed from the electrode and through tube 9 of a photo detector 38 and a light emitting device 39 was connected by wirebonding (refer to drawing 7 (b)). Here, the wire made from Au was used as a wire 40.

[0160] (4) Next, in the through tube 9 formed in the optical wiring layer, it was filled up with the resin constituent containing an epoxy resin, a silica particle (mean particle diameter: 0.5 micrometers), and a curing agent by printing to the same height as an optical element (a photo detector 38 and light emitting device 39), and lower layer resin packed bed 41a was formed by carrying out heat hardening of this resin constituent after that (refer to drawing 7 (c)).

[0161] Subsequently, it was filled up with the resin constituent containing silicone resin, a silica particle (mean particle diameter: 0.5 micrometers), and a curing agent by printing on lower layer resin packed bed 41a in a through tube 9, and buffing and mirror polishing were further given to the exposure of a resin constituent. Then, hardening processing was performed and it was referred to as upper resin packed bed 41b (refer to drawing 8 (a)). In addition, the permeability of the perpendicular direction of the wavelength the light of 0.85 micrometers between the top face and inferior surface of tongue of upper resin packed bed 41b is 93%.

[0162] (5) Next, the solder resist constituent prepared at the process of (15) of production of the above-mentioned package substrate and the same resin constituent were prepared, this was applied to the optical wiring layer side of a substrate, for 20 minutes was performed at 70 degrees C, desiccation processing was performed the condition for 30 minutes at 70 degrees C, and layer 54alpha of a solder REJISU constituent was formed. In addition, a solder resist constituent was not applied to the front face of upper resin packed bed 41b here. Subsequently, the photo mask with a thickness of 5mm with which the pattern of opening was drawn was stuck to layer 54alpha of a solder resist constituent, it exposed by the ultraviolet rays of 1000 mJ/cm2, the development was carried out with the DMTG solution, and opening 51 was formed. And further, it carried out at 120 degrees C for 1 hour for 1 hour, heat-treated [80 degrees C / 1 hour and 100 degrees C] on the conditions of 3 hours by 150 degrees C, respectively, layer 54alpha of a solder resist constituent was stiffened, and the solder resist layer 54 which has opening 51 was formed (refer to drawing 8 (b)). Therefore, when this process is finished, the solder resist layer 54 will be formed in an optical wiring layer side, and the solder resist layer 34 will be formed in the package substrate side, respectively.

[0163] (6) Next, the substrate in which the solder resist layer 54 was formed was immersed in the non-electrolyzed nickel-plating liquid of pH=4.5 containing a nickel chloride (2.3x10-1 mol/l), sodium hypophosphite (2.8x10-1 mol/l), and a sodium citrate (1.6x10 to 1 mol/l.) for 20 minutes, and the nickel-plating layer with a thickness of 5 micrometers was formed in a part of opening 51. Furthermore, the substrate was immersed in the non-electrolyzed gilding liquid containing a gold cyanide potassium (7.6x10-3 mol/l), an ammonium chloride (1.9x10-1 mol/l), a sodium citrate (1.2x10 to 1 mol/l.), and sodium hypophosphite (1.7x10-1 mol/l) for 7.5 minutes on 80-degree C conditions, and the gilding layer with a thickness of 0.03 micrometers was formed on the nickel-plating layer. In addition, all over drawing, two-layer [of a nickel-plating layer and a gilding layer] is doubled, and it is indicated as the metal layer 56.

[0164] (7) Next, soldering paste (Sn/Ag=96.5/3.5) was printed to the opening 31 which the solder resist layer 34 has, and the opening 51 formed in the solder resist layer 54, by carrying out a reflow at 250 degrees C, the solder bump 57 for flip chips and the solder bump 58 for BGA were formed, and the substrate for IC chip mounting was obtained (refer to drawing 8 (c)).

[0165] (Example 2)

A. Production of the resin film for the resin insulating layers between layers and preparation of a resin filler were performed like (a) of A of production of the resin film for the resin insulating layers between the (production a) layers, and the preparation example 1 of a resin filler, and (b). [of a package substrate]

[0166] (b) Double-sided copper clad laminate which 18-micrometer copper foil 28 laminates to both sides of the insulating substrate 21 which consists of the glass epoxy resin with a manufacture (1) thickness of 0.8mm or BT (bismaleimide triazine) resin of a package substrate was used as the start ingredient (refer to drawing 9 (a)).

first, the thing which drill drilling of this copper clad laminate is carried out, and nonelectrolytic plating processing is performed, and is etched in the shape of a pattern — both sides of a substrate — a lower layer — a conductor — the circuit 24 and the through hole 29 were formed (refer to drawing 9 (b)).

[0167] (2) a lower layer — a conductor — washing in cold water the substrate 21 in which the circuit 24 was formed, and, after drying Melanism processing the water solution containing NaOH (10g/(l.)), NaClO2 (40 g/l), and Na3PO4 (6 g/l) — melanism — it considers as a bath (oxidation bath) — and the reduction processing which makes a reduction bath NaOH (10 g/l) and the water solution containing NaBH4 (6 g/l) — carrying out — a lower layer — a conductor — the roughening side (not shown) was formed in the front face of a circuit 24.

[0168] (3) next, the following approach after preparing the resin filler indicated above (a) — after preparation — less than 24 hours — the conductor of one side of the inside of a through hole 29, and a substrate 21 — the circuit agenesis section and a lower layer — a conductor — the layer of resin filler 30' was formed in the rim section of a circuit 24. That is, after pushing in a resin filler in a through hole using a squeegee, it was made to dry on 100 degrees C and the conditions for 20 minutes first. next, a conductor — the conductor with which the part equivalent to the circuit agenesis section lays on a substrate the mask which carried out opening, and serves as a crevice using the squeegee — the circuit agenesis section was also filled up with the resin filler, and the layer of resin filler 30' was formed by making it dry on 100 degrees C and the conditions for 20 minutes (refer to drawing 9 R> 9 (c)).

[0169] (4) the belt sander [one side / which finished processing of the above (3) / of a substrate] polish using the belt abrasive paper (Sankyo Rikagaku make) of **600 — a conductor — it ground so that resin filler 30' might remain neither in the front face of a circuit 24, nor the land front face of a through hole 29, and subsequently buffing for removing the blemish by the above-mentioned belt sander polish was performed. Such a series of processings were similarly performed about the field of another side of a substrate. Subsequently, by 100 degrees C, it performed at 150 degrees C for 1 hour for 3 hours, 120 degrees C performed heat-treatment of 7 hours at 180 degrees C for 1 hour, and the resin filler layer 30 was formed.

[0170] Flattening of the front face of a circuit 24 is carried out. thus, a through hole 29 and a conductor — the surface section of the resin filler layer 30 formed in the circuit agenesis section, and a conductor — the resin filler layer 30 and a conductor — the insulating substrate which the side face of a circuit 24 stuck firmly through the roughening side (not shown), and the internal surface and the resin filler layer 30 of a through hole 29 stuck firmly through the roughening side (not shown) was obtained (refer to drawing 9 (d)). this process — the front face of the resin filler layer 30, and a conductor — the front face of a circuit 24 turns into the same flat surface.

[0171] (5) software etching after rinsing and carrying out acid cleaning of the above-mentioned substrate — carrying out — subsequently — an etching reagent — both sides of a substrate — a spray — spraying — a conductor — etching the front face of a circuit 24, and the land front face of a through hole 29 — a conductor — the roughening side (not shown) was formed in all the front faces of a circuit 24. In addition, as an etching reagent, the product made from MEKKU and MEKKU dirty bond were used.

[0172] (6) Next, by 0.5MPa, it laminated vaccum pressure arrival, the resin film for the resin insulating layers between layers produced above (a) was stuck, carrying out a temperature up to the temperature of 50-150 degrees C, and resin film layer 22alpha was formed (refer to drawing 9 (e)).

[0173] (7) Next, through the mask with which the through tube with a thickness of 1.2mm was formed on resin film layer 22alpha, on the beam diameter of 4.0mm, the Top Hat mode, 8.0 microseconds of pulse width, the path of 1.0mm of the through tube of a mask, and the conditions of one shot, the opening 26 for the Bahia halls with a diameter of 80 micrometers was formed in resin film layer 22alpha, and it considered as the resin insulating layer 22 between layers in CO2 gas laser with a wavelength of 10.4 micrometers (refer to drawing 1010 (a)).

[0174] (8) The roughening side (not shown) was formed in the front face of the resin insulating layer 22 between layers containing the internal surface of the opening 26 for the Bahia halls by immersing the substrate in which the opening 26 for the Bahia halls was formed, for 10 minutes in the 80-degree C solution containing 60g [/l.] permanganic acid, and carrying out dissolution removal of the epoxy resin particle which exists in the front face of the resin insulating layer 22 between layers.

[0175] (9) Next, the substrate which finished the above-mentioned processing was washed in cold water after being immersed in the neutralization solution (product made from SHIPUREI). Furthermore, the catalyst nucleus was made for the front face of this substrate that carried out the surface roughening process (a roughening depth of 3 micrometers) to adhere to the front face (for the internal surface of the opening 26 for the Bahia halls to be included) of the resin insulating layer 22 between layers by giving a palladium catalyst (not shown). That is, the above-mentioned substrate was immersed into the catalytic liquid containing a palladium chloride (PdCl2) and a stannous chloride (SnCl2), and the catalyst was given by depositing a palladium metal.

[0176] (10) Next, a substrate is immersed into the nonelectrolytic plating liquid used at the process of (10) of

production of the package substrate of an example 1, and the non-electrolytic copper plating liquid of the same presentation. The non-electrolytic copper plating film (thin film conductor layer) 32 with a thickness of 0.6-3.0 micrometers was formed in the front face (the internal surface of the opening 26 for the Bahia halls is included) of the resin insulating layer 22 between layers by processing on the same conditions (refer to drawing 10 (b)).
[0177] (11) Next, plating resist 23 was formed by sticking a commercial photosensitive dry film on the substrate with which the non-electrolytic copper plating film 32 was formed, laying a mask, exposing by 100 mJ/cm2, and carrying out a development in a sodium-carbonate water solution 0.8% (refer to drawing 10 (c)).
[0178] 50-degree C water washes a substrate and it degreases. With 25-degree C water (12) Subsequently, after rinsing, By immersing a substrate into the electrolysis plating liquid used at the process of (12) of production of the package substrate of an example 1, and the electrolysis plating liquid of the same presentation, and processing on the same conditions, after a sulfuric acid furthermore washes The electrolytic copper plating film 33 was formed in the plating-resist 23 agenesis section (refer to drawing 10 (d)).
[0179] (13) — the nonelectrolytic plating film under the plating resist 23 after carrying out exfoliation removal of the plating resist 23 by KOH 5% further — the mixed liquor of a sulfuric acid and a hydrogen peroxide — etching processing — carrying out — dissolution removal — carrying out — the upper layer — a conductor — it considered as the circuit 25 (the Bahia hall 27 is included) (refer to drawing 11 (a)).
[0180] (14) next, the upper layer — a conductor — the substrate in which the circuit 25 grade was formed — an etching reagent — being immersed — the upper layer — a conductor — the roughening side (not shown) was formed in the front face of a circuit 25 (the Bahia hall 27 is included). In addition, as an etching reagent, the product made from MEKKU and MEKKU dirty bond were used.
[0181] (15) Next, the solder resist constituent was prepared like the process of (15) of production of the package substrate of an example 1.
(16) next, the upper layer — a conductor — the above-mentioned solder resist constituent was applied, for 20 minutes was performed at 70 degrees C, desiccation processing was performed to both sides of the substrate in which the circuit 25 grade was formed, the condition for 30 minutes at 70 degrees C, and layer 34alpha of a solder REJISU constituent was formed in them (refer to drawing 11 (b)). Subsequently, the photo mask with a thickness of 5mm with which the pattern of opening was drawn was stuck to layer 34alpha of a solder resist constituent, it exposed by the ultraviolet rays of 1000 mJ/cm2, the development was carried out with the DMTG solution, and opening 31 was formed. And further, it carried out at 120 degrees C for 1 hour for 1 hour, heat-treated [80 degrees C / 1 hour and 100 degrees C] on the conditions of 3 hours by 150 degrees C, respectively, layer 34alpha of a solder resist constituent was stiffened, and the solder resist layer 34 which has opening 31 was formed (refer to drawing 11 (c)).
[0182] (17) Next, the substrate in which the solder resist layer 34 was formed was immersed in the non-electrolyzed nickel-plating liquid of pH=4.5 containing a nickel chloride (2.3x10-1 mol/l), sodium hypophosphite (2.8x10-1 mol/l), and a sodium citrate (1.6x10-1 mol/l) for 20 minutes, and the nickel-plating layer was formed in a part of opening 31. Furthermore, the substrate was immersed in the non-electrolyzed gilding liquid containing a gold cyanide potassium (7.6x10-3 mol/l), an ammonium chloride (1.9x10-1 mol/l), a sodium citrate (1.2x10-1 mol/l), and sodium hypophosphite (1.7x10-1 mol/l) for 7.5 minutes on 80-degree C conditions, the gilding layer was formed on the nickel-plating layer, and it considered as the package substrate (refer to drawing 11 (d)). In addition, all over drawing, two-layer [of a nickel-plating layer and a gilding layer] is doubled, and it is indicated as the metal layer 36.
[0183] B. One side copper clad laminate which 18-micrometer copper foil 8 laminates on one side of the insulating substrate 1 which consists of the glass epoxy resin with a production (1) thickness of 0.8mm or BT (bismaleimide triazine) resin of an optical wiring layer was used as the start ingredient (refer to drawing 12 (a)). first, the thing for which the copper foil 8 of this one side copper clad laminate is etched in the shape of a pattern — one side of a substrate — a conductor — the circuit 4 was formed (refer to drawing 12 (b)).
[0184] (2) next, the conductor of a substrate — the side in which the circuit 4 was formed — a conductor — the adhesives layer (not shown) was formed by applying epoxy resin adhesive to the circuit agenesis section.
(3) Further, the through tube 9 was formed in the center section of a substrate by router processing, and it considered as the optical wiring layer (refer to drawing 12 (c)).
[0185] C. The laminating press by the production (1) mass lamination method of the substrate for IC chip mounting was performed, and the substrate which stuck the package substrate produced by Above A and the optical wiring layer produced by Above B through the adhesives layer formed in the above-mentioned optical wiring layer was obtained (refer to drawing 13 (a)). That is, after performing both alignment, a temperature up is carried out to 150 degrees C, and the optical wiring layer and the package substrate were stuck by pressing in a pan by the pressure of 5MPa(s).
[0186] (2) Next, the photo detector 38 and the light emitting device 39 were attached in the front face of the

package substrate exposed from the through tube 9 formed in the optical wiring layer using the silver paste so that light sensing portion 38a and light-emitting part 39a might be up exposed, respectively. In addition, as a photo detector 38, what consists of InGaAsP was used as a light emitting device 39 using what consists of InGaAs.

[0187] (3) Next, the metal layer 36 of the front face of the package substrate exposed from the electrode and through tube 9 of a photo detector 38 and a light emitting device 39 was connected by wirebonding (refer to drawing 13 (b)). Here, the wire made from Au was used as a wire 40.

[0188] (4) Next, in the through tube 9 formed in the optical wiring layer, it was filled up with the resin constituent containing an epoxy resin, a silica particle (mean particle diameter: 0.5 micrometers), and a curing agent by printing to the same height as an optical element (a photo detector 38 and light emitting device 39), and lower layer resin packed bed 41a was formed by carrying out heat hardening of this resin constituent after that (refer to drawing 13 (c)).

[0189] Subsequently, it was filled up with the resin constituent containing silicone resin, a silica particle (mean particle diameter: 0.5 micrometers), and a curing agent by printing on lower layer resin packed bed 41a in a through tube 9, and buffing and mirror polishing were further given to the exposure of a resin constituent. Then, hardening processing was performed and it was referred to as upper resin packed bed 41b (refer to drawing 14 (a)). In addition, the permeability of the perpendicular direction of the wavelength the light of 0.85 micrometers between the top face and inferior surface of tongue of upper resin packed bed 41b is 93%.

[0190] (5) Next, the through tube 46 with a diameter of 400 micrometers which penetrates an optical wiring layer and a package substrate was formed by drilling (refer to drawing 14 (b)). Furthermore, DESUMIA processing was performed to the wall surface of a through tube 46 by being immersed in the 80-degree C solution containing the permanganic acid of 60 g/l for 10 minutes.

[0191] (6) Next, the substrate which finished the above-mentioned processing was washed in cold water after being immersed in the neutralization solution (product made from SHIPUREI). Furthermore, the catalyst nucleus was made to adhere to the wall surface of a through tube 46 etc. by giving a palladium catalyst to the exposure of the optical wiring layer containing the wall surface of a through tube 46, and a package substrate (not shown).

[0192] (7) Next, the substrate was immersed into the non-electrolytic copper plating water solution, and the non-electrolytic copper plating film (thin film conductor layer) 52 with a thickness of 0.6-3.0 micrometers was formed in the exposure of the optical wiring layer containing the wall surface of a through tube 46, and a package substrate. In addition, it processed on the same conditions using the same thing as the nonelectrolytic plating liquid used at the process of (10) at the time of producing a package substrate as nonelectrolytic plating liquid.

[0193] (8) Next, plating resist 43 was formed by sticking a commercial photosensitive dry film on the substrate with which the non-electrolytic copper plating film 52 was formed, laying a mask, exposing by 100 mJ/cm2, and carrying out a development in a sodium-carbonate water solution 0.8% (refer to drawing 14 (c)).

[0194] (9) Subsequently, 50-degree C water washed the substrate and it degreased, and with 25-degree C water, after rinsing, after the sulfuric acid washed further, electrolysis plating was performed, and the electrolytic copper plating film 53 was formed in the plating-resist 43 agenesis section (refer to drawing 15 (a)). In addition, it processed on the same conditions using the same thing as the electrolysis plating liquid used at the process of (12) at the time of producing a package substrate as electrolysis plating liquid.

[0195] (10) Further, after carrying out exfoliation removal of the plating resist 43 by KOH 5%, etching processing of the nonelectrolytic plating film under the plating resist 43 was carried out with the mixed liquor of a sulfuric acid and a hydrogen peroxide, and dissolution removal was carried out and it considered as the through hole 49 which penetrates an optical wiring layer and a package substrate (refer to drawing 15 (b)).

[0196] (11) Next, the substrate in which the through hole 49 was formed was immersed in the etching reagent (the product made from MEKKU, MEKKU dirty bond), and the roughening side (not shown) was formed in through hole 49 wall surface (the front face of a land part is included). Next, after preparing the same resin constituent as the resin filler indicated to (b) of production of the above-mentioned package substrate, the layer of a resin filler was formed in the through hole 49 within 24 hours after preparation by the following approach. That is, after pushing in a resin filler in a through hole 49 using a squeegee, the layer of a resin filler was formed by making it dry on 100 degrees C and the conditions for 20 minutes.

[0197] Furthermore, by belt sander polish using the belt abrasive paper (Sankyo Rikagaku make) of **600, it ground so that a resin filler might not remain in the land front face of a through hole 49, and subsequently buffing for removing the blemish by the above-mentioned belt sander polish was performed. Furthermore, by 100 degrees C, it performed at 150 degrees C for 1 hour for 3 hours, 120 degrees C performed heat-treatment of 7 hours at 180 degrees C for 1 hour, and the exposure from the through hole formed the flat resin filler layer 50 (refer to drawing 15 (c)).

[0198] (12) Next, the solder resist constituent prepared at the process of (15) of production of the above-

mentioned package substrate and the same resin constituent were prepared, this was applied to both sides of a substrate, for 20 minutes was performed at 70 degrees C, desiccation processing was performed the condition for 30 minutes at 70 degrees C, and layer 54alpha of a solder REJISU constituent was formed (refer to drawing 16 (a)). In addition, a solder resist constituent was not applied to the front face of the resin packed bed 41 here. Subsequently, the photo mask with a thickness of 5mm with which the pattern of opening was drawn was stuck to layer 54alpha of a solder resist constituent, it exposed by the ultraviolet rays of 1000 mJ/cm2, the development was carried out with the DMTG solution, and opening 51 was formed. And further, it carried out at 120 degrees C for 1 hour for 1 hour, heat-treated [80 degrees C / 1 hour and 100 degrees C] on the conditions of 3 hours by 150 degrees C, respectively, layer 54alpha of a solder resist constituent was stiffened, and the solder resist layer 54 which has opening 51 was formed (refer to drawing 16 (b)).

[0199] (13) Next, the substrate in which the solder resist layer 54 was formed was immersed in the non-electrolyzed nickel-plating liquid of pH=4.5 containing a nickel chloride (2.3x10-1 mol/l), sodium hypophosphite (2.8x10-1 mol/l), and a sodium citrate (1.6x10 to 1 mol/l.) for 20 minutes, and the nickel-plating layer with a thickness of 5 micrometers was formed in a part of opening 51. Furthermore, the substrate was immersed in the non-electrolyzed gilding liquid containing a gold cyanide potassium (7.6x10-3 mol/l), an ammonium chloride (1.9x10-1 mol/l), a sodium citrate (1.2x10 to 1 mol/l.), and sodium hypophosphite (1.7x10-1 mol/l) for 7.5 minutes on 80-degree C conditions, and the gilding layer with a thickness of 0.03 micrometers was formed on the nickel-plating layer. In addition, all over drawing, two-layer [of a nickel-plating layer and a gilding layer] is doubled, and it is indicated as the metal layer 56.

[0200] (14) Next, soldering paste (Sn/Ag=96.5/3.5) was printed to the opening 51 formed in the solder resist layer 54, by carrying out a reflow at 250 degrees C, the solder bump 57 for flip chips and the solder bump 58 for BGA were formed, and the substrate for IC chip mounting was obtained (refer to drawing 16 R> 6 (c)).

[0201] thus, about each substrate for IC chip mounting of the acquired examples 1 and 2 Mount IC chip by flip chip mounting, and the end face of an optical fiber is further arranged in the location which counters the light sensing portion of a photo detector. After attaching the detector in the location which counters the light-emitting part of a light emitting device and making a lightwave signal calculate with delivery and IC chip through an optical fiber after that, when the detector detected the lightwave signal, the substrate for IC chip mounting of examples 1 and 2 was able to detect the desired lightwave signal.

[0202]

[Effect of the Invention] As explained above, since the optical element is mounted in that interior, when the substrate for IC chip mounting of this invention mounts IC chip in this substrate for IC chip mounting, the distance of IC chip and an optic is short and excellent in the dependability of electrical signal transmission. Moreover, in the above-mentioned substrate for IC chip mounting, since electronic parts and an optic required for optical communication are unified, the miniaturization of the terminal equipment for optical communication can be attained.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing typically 1 operation gestalt of the substrate for IC chip mounting of this invention.
[Drawing 2] It is the sectional view showing typically 1 another operation gestalt of the substrate for IC chip mounting of this invention.
[Drawing 3] (a) – (e) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 4] (a) – (d) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 5] (a) – (d) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 6] (a) – (g) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 7] (a) – (c) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 8] (a) – (c) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 9] (a) – (e) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 10] (a) – (d) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 11] (a) – (d) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 12] (a) – (c) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 13] (a) – (c) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 14] (a) – (c) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 15] (a) – (c) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Drawing 16] (a) – (c) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting of this invention.
[Description of Notations]
1 21 Insulating substrate
8 28 Copper foil
4 and 24 a lower layer — a conductor — circuit
6 29 Through hole
9 Through Tube
10 30 Resin filler layer
12 Conductor Layer
14 Conductor Layer
16 Lid Plating Layer
22 Resin Insulating Layer between Layers
23 Plating Resist

25 Conductor — Circuit
27 Bahia Hall
32 Thin Film Conductor Layer
33 Electrolysis Plating Film
34 54 Solder resist layer
36 56 Metal layer
38 Photo Detector
39 Light Emitting Device
40 Wire
41 Resin Packed Bed
57 Solder Bump for Flip Chips
58 Solder Bump for BGA
100,200 Substrate for IC chip mounting
120 220 Gilding layer
160 260 Package substrate
180 280 IC chip
1238 1239 Pad for connection

[Translation done.]